

UMA & Optimus Schematics Document

IVY Bridge(rPGA989)

Intel PCH(Panther Point)

DY :NotInstalled

UMA:UMA platform installed

OPS:Optimus

HR:Huron River

CR:Chief River

V: V-Series installed

<Core Design>

緯創資通

Wistron Corporation

21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title

Cover Page

Size

A4

Document Number

LA480

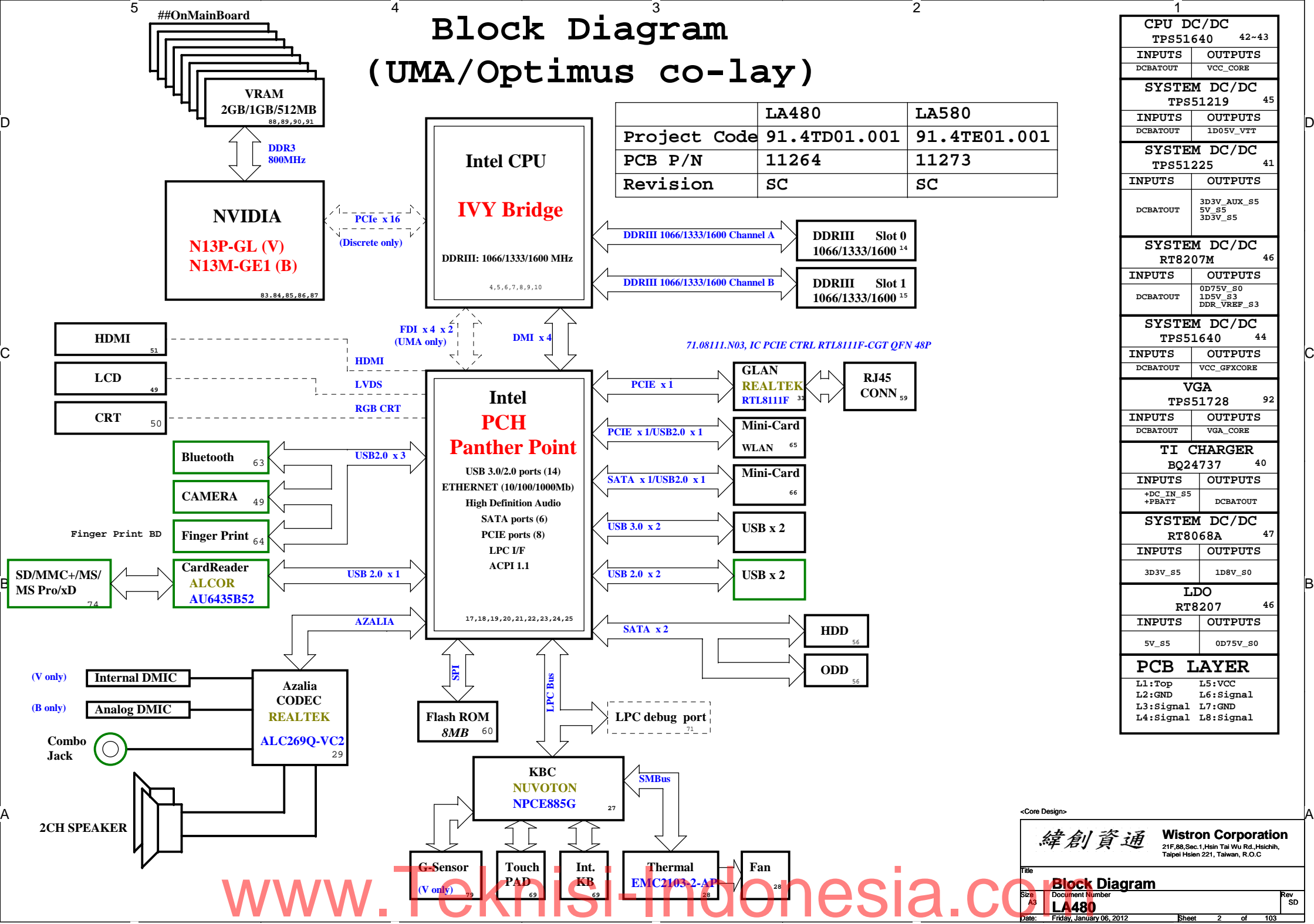
Rev

SD

Date: Friday, January 06, 2012

Sheet 1 of 103

Block Diagram (UMA/Optimus co-lay)



<Core Design>

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Date

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Block Diagram

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LA480

Sheet

2

of

103

Rev

SD

PCH Strapping Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIe Routing

LANE1	X
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	Intel GBE LAN / LAN
LANE7	X
LANE8	Express Card

USB Table port9 is debug port

Pair	Device
0	USB3.0 ext port 1
1	USB3.0 ext port 2
2	USB3.0 ext port 3
3	USB3.0 ext port 4
4	BLUETOOTH (USB1.1)
5	Fingerprint (USB1.1)
6	X
7	X
8	Mini Card2 (WWAN)
9	USB ext. port 4 / E-SATA /USB CHARGER
10	CARD READER
11	Mini Card1 (WLAN)
12	CCD
13	New Card

Processor Strapping Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is 0: connect to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	DESCRIPTION
		ACTIVE IN	
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D0V_VTT 1D0V_S0 VCCSA UD75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

SMBus ADDRESSES

I 2 C / SMBus Addresses	Ref Des	Chief River CRV
Device	Address	Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

<Core Design>

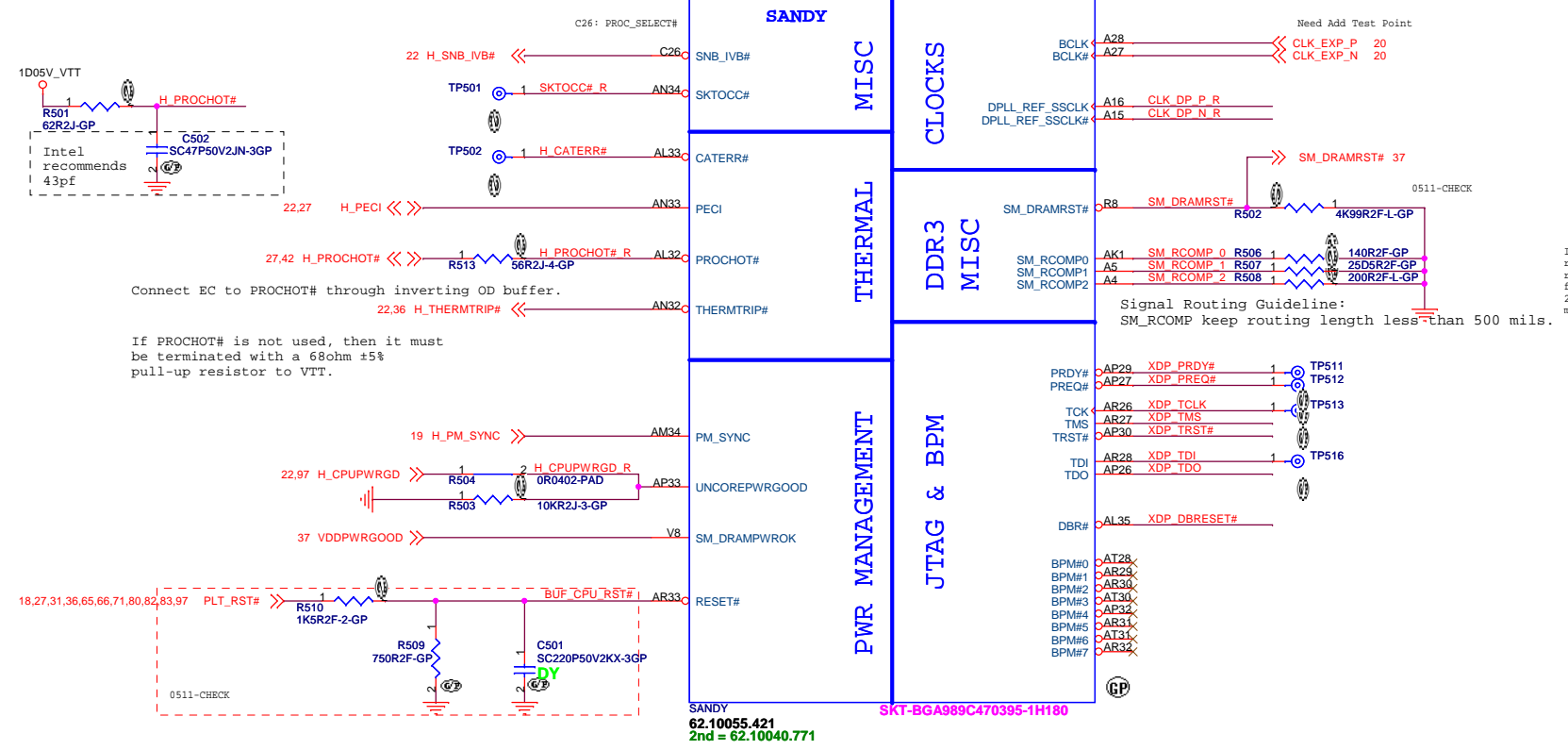
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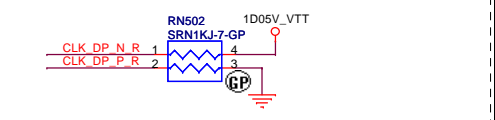
Size A3 Document Number **LA480** Rev SD

Date: Friday, January 06, 2012 Sheet 3 of 103

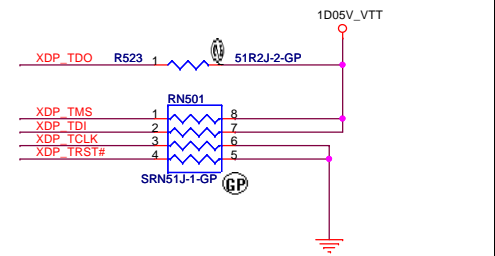
SSID = CPU



Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K $\pm 5\%$ resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K $\pm 5\%$ resistor power (~15 mW) may be wasted.

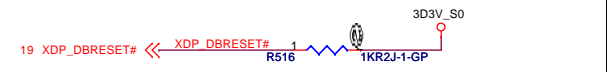


In order to minimize resistance, use thick traces to route all COMP signals, use 10-mils wide trace for routing less than 500 mils, or 20-mils wide trace for routing between 500 mils and 1000 mils. Keep 20-mils spacing to any other signals in order to minimize crosstalk.

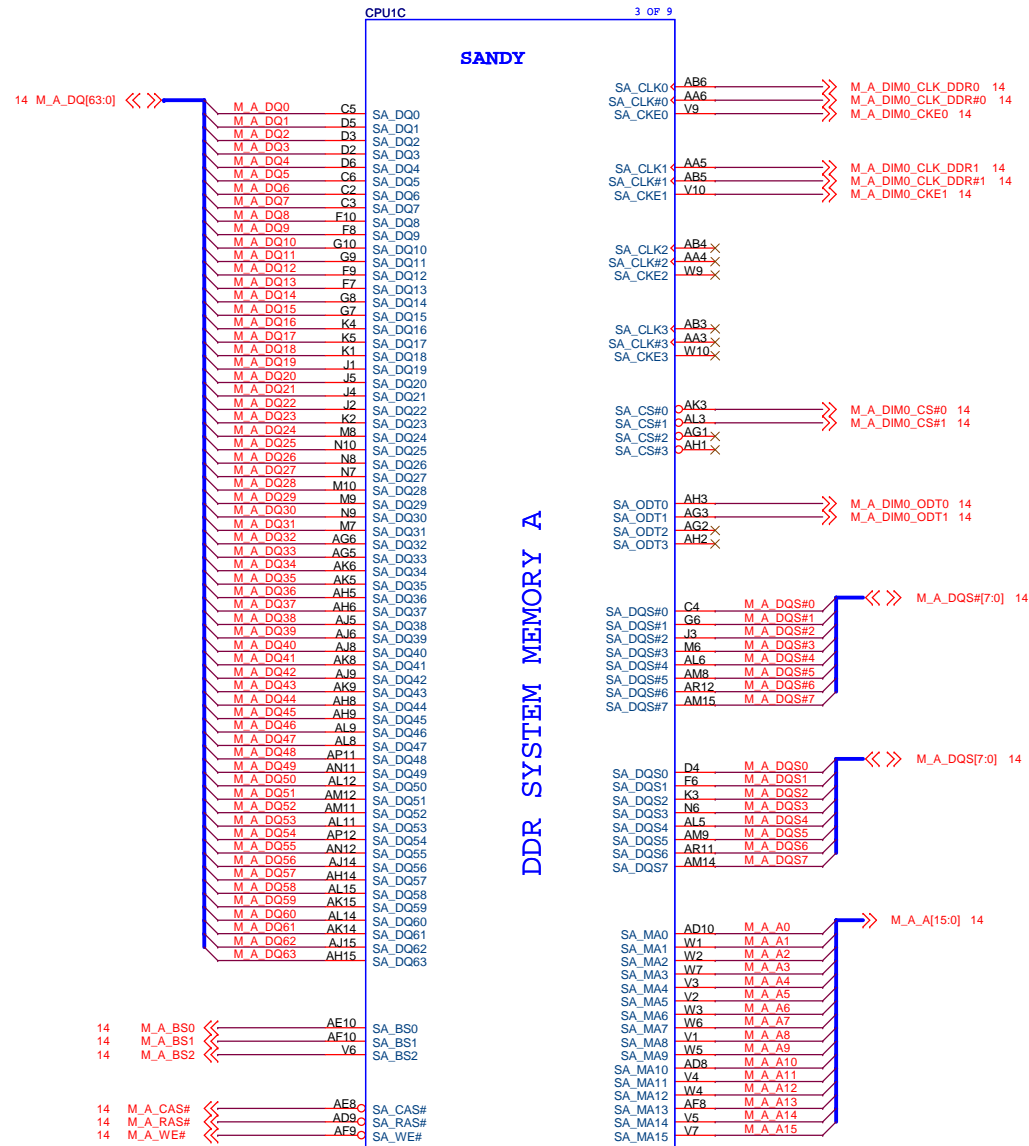


DEL U501
DEL R519
DEL C503
DEL R517
DEL R515

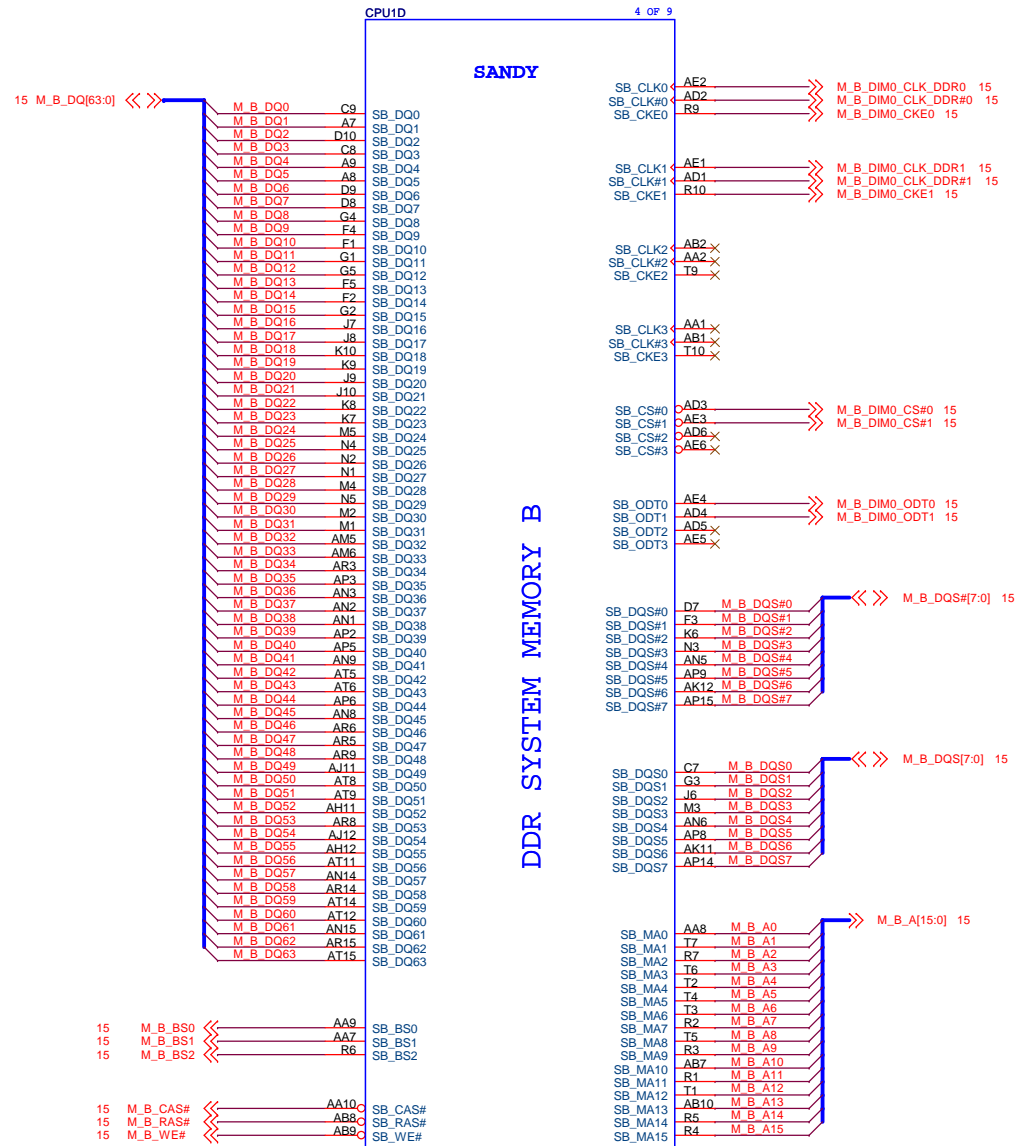
ASM R510
ASM R509



SSID = CPU



SANDY
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2nd = 62.10040.771



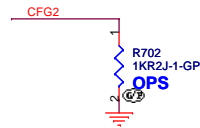
SANDY
62.10055.421
2nd = 62.10040.771

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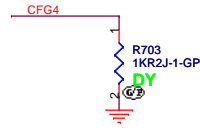
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Size	Document Number	Rev	SD
A3	LA480		
Date:	Friday, January 06, 2012	Sheet	6 of 103

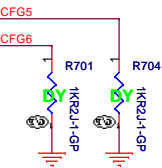
SSID = CPU



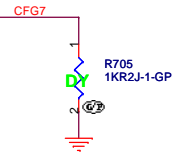
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



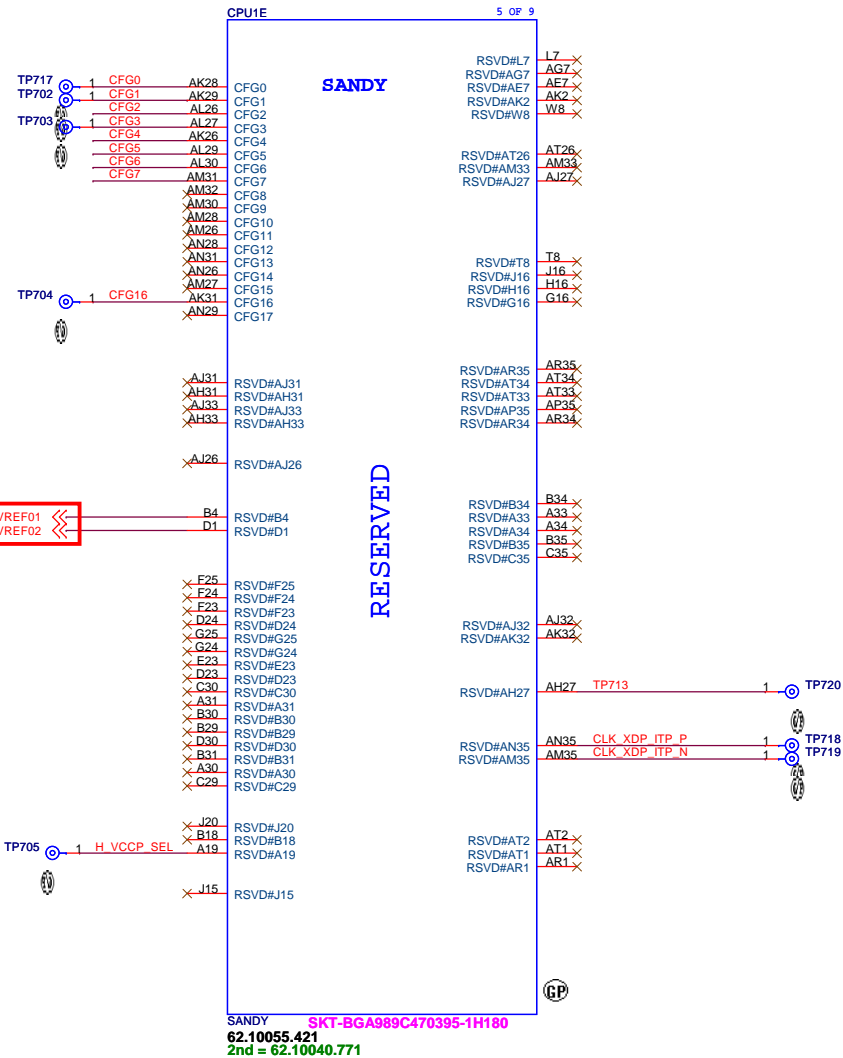
Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



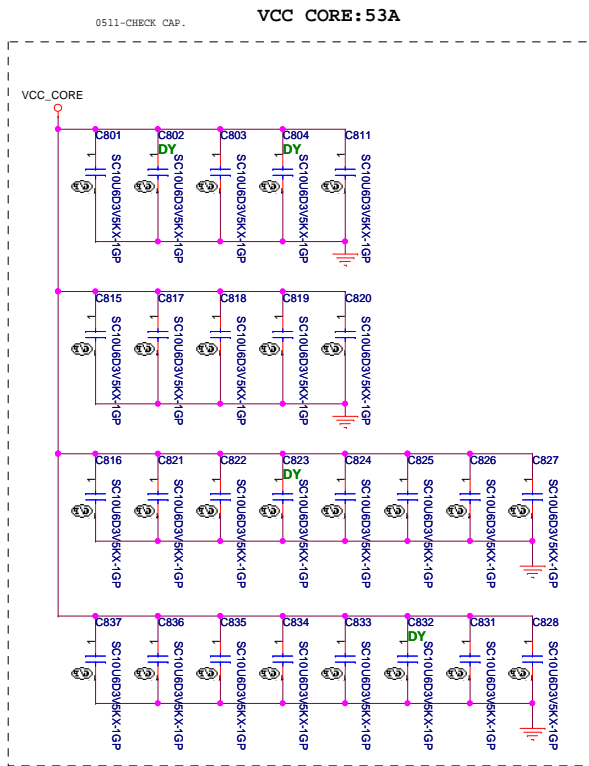
PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



SANDY
62.10055.421
2nd = 62.10040.771



VCC_CORE

AG35 VCC
AG34 VCC
AG33 VCC
AG32 VCC
AG31 VCC
AG30 VCC
AG29 VCC
AG28 VCC
AG27 VCC
AG26 VCC
AF35 VCC
AF34 VCC
AF33 VCC
AF32 VCC
AF31 VCC
AF30 VCC
AF29 VCC
AF28 VCC
AF27 VCC
AD35 VCC
AD34 VCC
AD33 VCC
AD32 VCC
AD31 VCC
AD30 VCC
AD29 VCC
AD28 VCC
AD27 VCC
AD26 VCC
AC35 VCC
AC34 VCC
AC33 VCC
AC32 VCC
AC31 VCC
AC30 VCC
AC29 VCC
AC28 VCC
AC27 VCC
AC26 VCC
AA35 VCC
AA34 VCC
AA33 VCC
AA32 VCC
AA31 VCC
AA30 VCC
AA29 VCC
AA28 VCC
AA27 VCC
AA26 VCC
Y35 VCC
Y34 VCC
Y33 VCC
Y32 VCC
Y31 VCC
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Y12 VCC
Y11 VCC
Y10 VCC
Y9 VCC
Y8 VCC
Y7 VCC
Y6 VCC
Y5 VCC
Y4 VCC
Y3 VCC
Y2 VCC
Y1 VCC
U35 VCC
U34 VCC
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U25 VCC
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U21 VCC
U20 VCC
U19 VCC
U18 VCC
U17 VCC
U16 VCC
U15 VCC
U14 VCC
U13 VCC
U12 VCC
U11 VCC
U10 VCC
U9 VCC
U8 VCC
U7 VCC
U6 VCC
U5 VCC
U4 VCC
U3 VCC
U2 VCC
U1 VCC
P35 VCC
P34 VCC
P33 VCC
P32 VCC
P31 VCC
P30 VCC
P29 VCC
P28 VCC
P27 VCC
P26 VCC

CORE SUPPLY

PEG AND DDR

POWER

SENSE LINES

SVID

VIDALERT#
VIDCLK
VIDSOUT

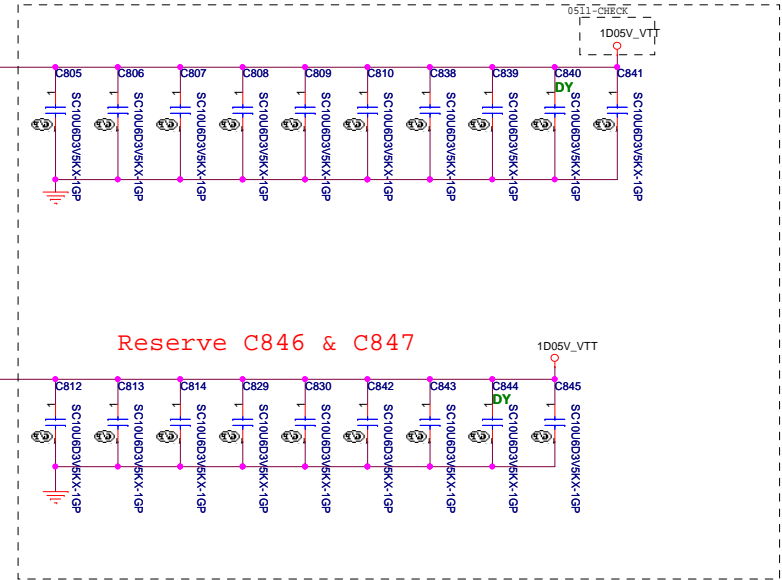
VCC_SENSE
VSS_SENSE

VCCIO_SENSE
VSSIO_SENSE

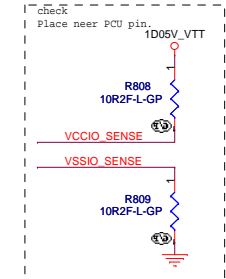
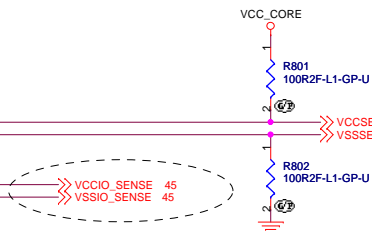
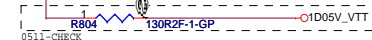
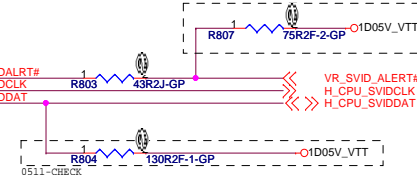
VCCIO AH13
VCCIO AH10
VCCIO AG10
VCCIO Y10
VCCIO U10
VCCIO P10
VCCIO L10
VCCIO J14
VCCIO J13
VCCIO J12
VCCIO J11
VCCIO H14
VCCIO H12
VCCIO H11
VCCIO G14
VCCIO G13
VCCIO G12
VCCIO F14
VCCIO F13
VCCIO F12
VCCIO F11
VCCIO E14
VCCIO E12
VCCIO E11
VCCIO D14
VCCIO D13
VCCIO D12
VCCIO D11
VCCIO C14
VCCIO C13
VCCIO C12
VCCIO C11
VCCIO B14
VCCIO B12
VCCIO A14
VCCIO A13
VCCIO A12
VCCIO A11
VCCIO J23

(GP)

0511-CHECK CAP. VCCIO:8.5A



For CRB VIDSOUT need to pull high 130 ohm closer to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU



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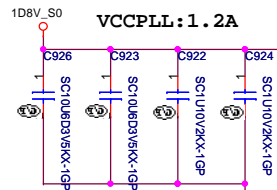
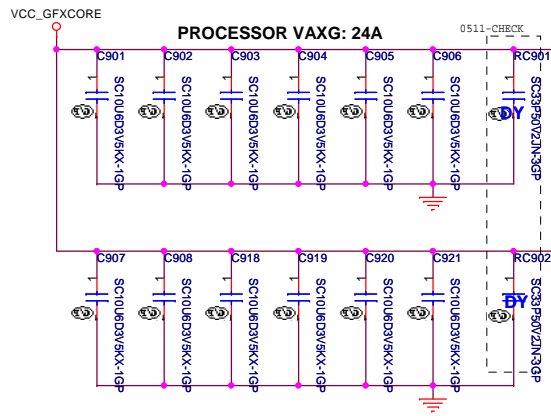
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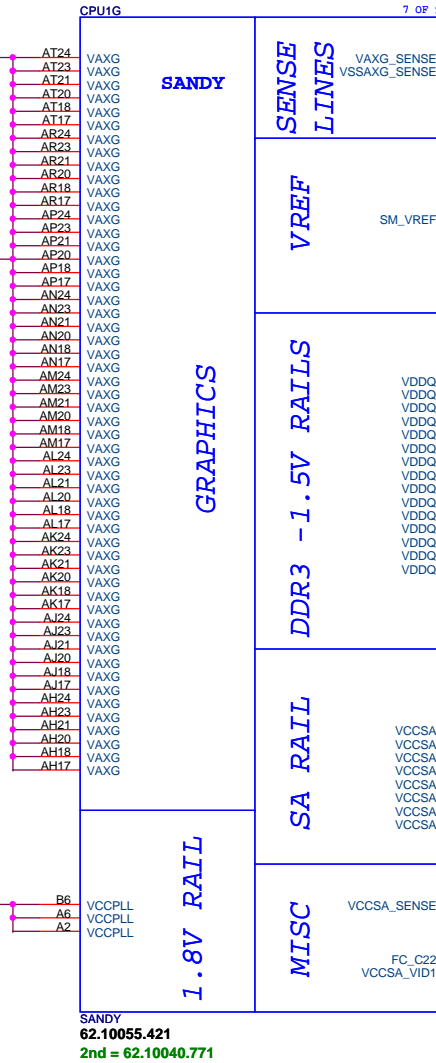
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Date: Friday, January 06, 2012 Sheet 8 of 103

0511-CHECK CAP



POWER



Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

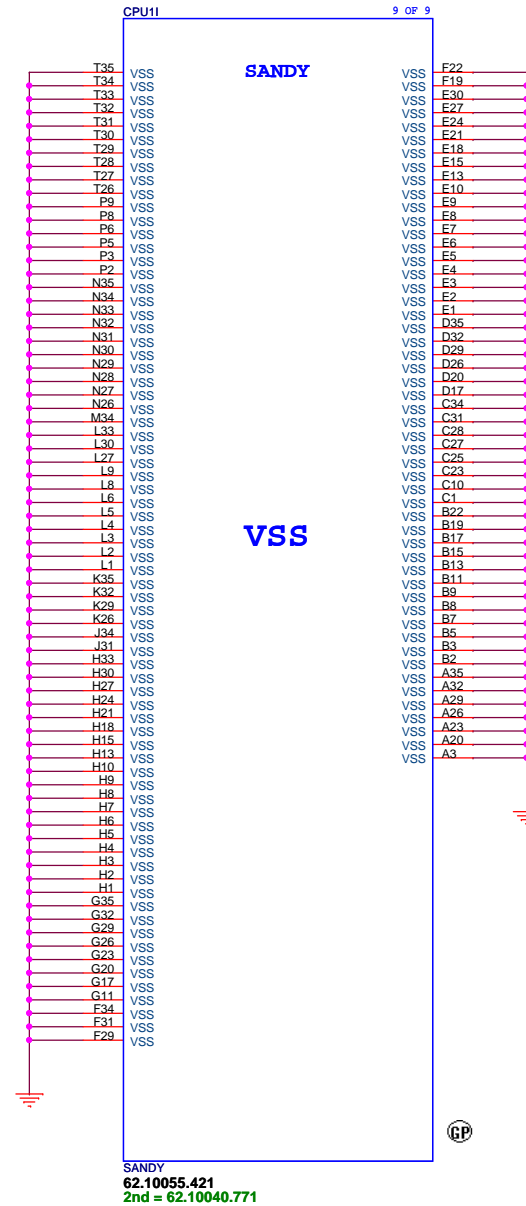
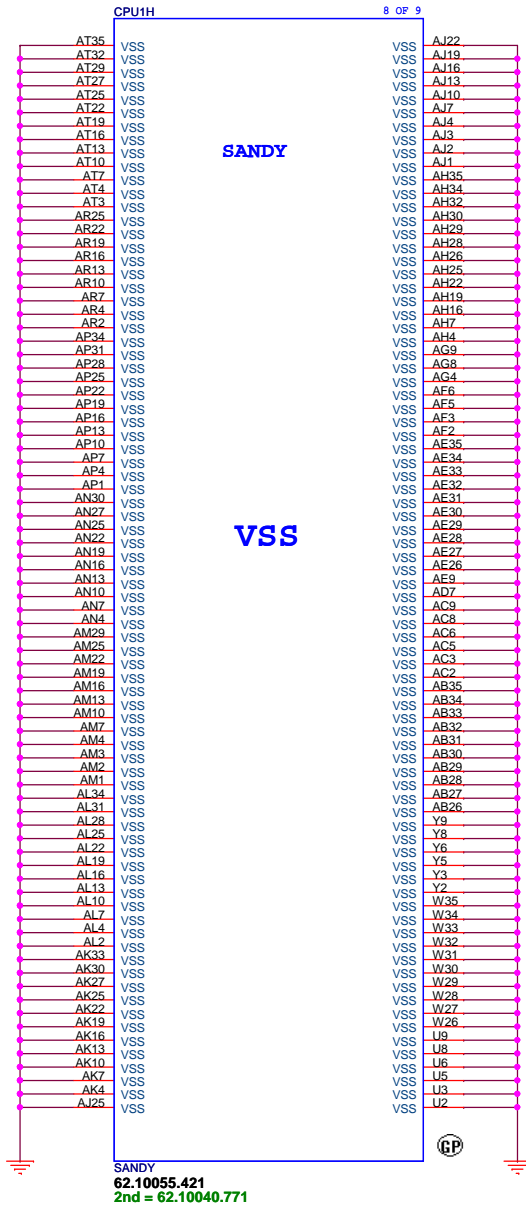
+V0.85S - VCCSA - System Agent rail voltage can be [0.9, 0.725, 0.8, 0.675] V for IVB
[0.9, 0.8] V for SNB

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Title CPU (VCC GFXCORE)
Size A3 Document Number LA480 Rev SD
Date: Friday, January 06, 2012 Sheet 9 of 103

SSID = CPU



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Title			CPU (VSS)
Size	Document Number	Rev	
A3	LA480	SD	
Date:	Friday, January 06, 2012	Sheet	10 of 103

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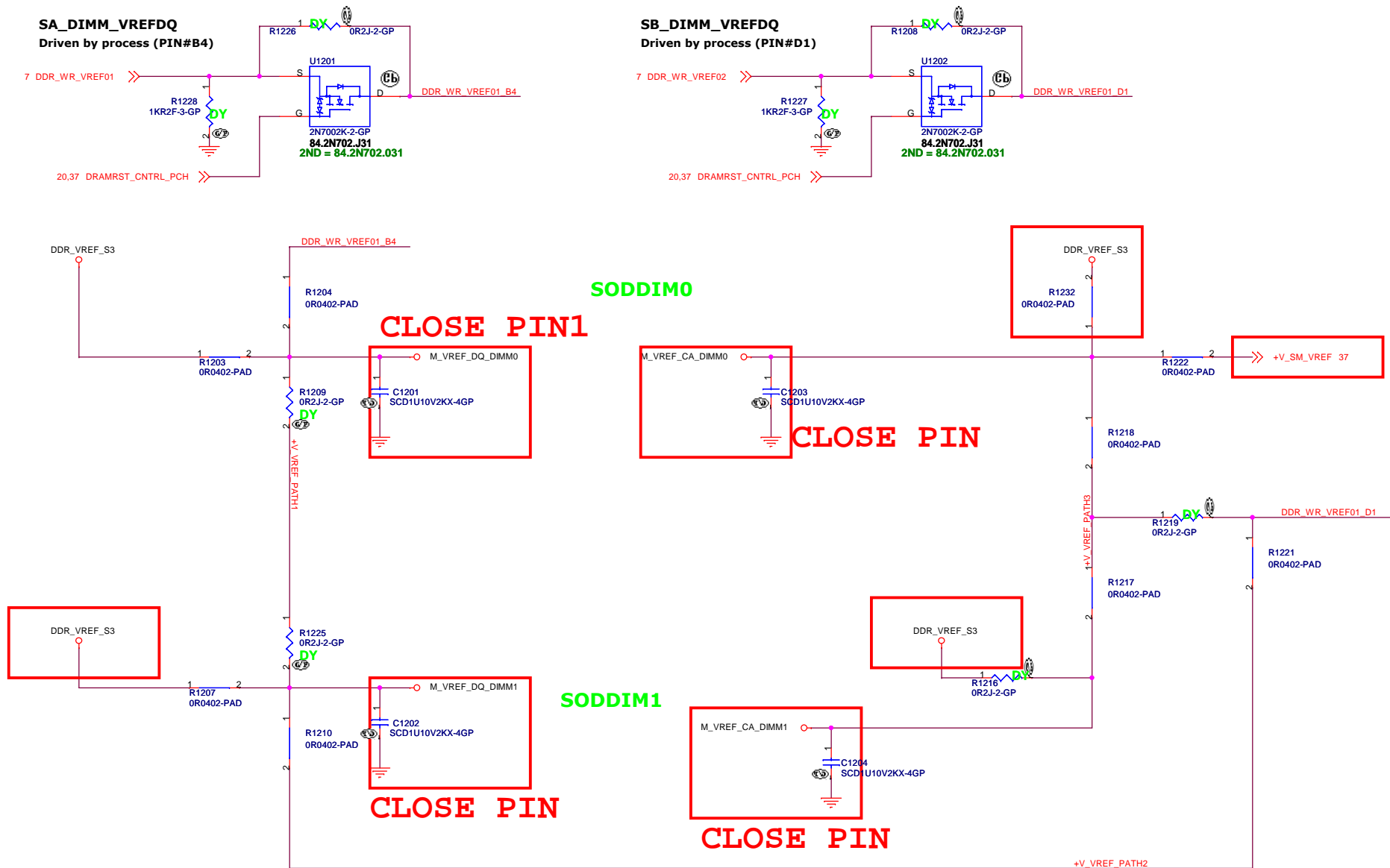
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VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

CAD Note: All VREF traces should have 20:20 mil trace geometry. Note that while 20 mil trace width is optimal, short violations are acceptable if required due to tight routing constraints.



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Title	M3		
Size	Document Number	Rev	
A3	LA480	SD	
Date:	Friday, January 06, 2012	Sheet	12 of 103

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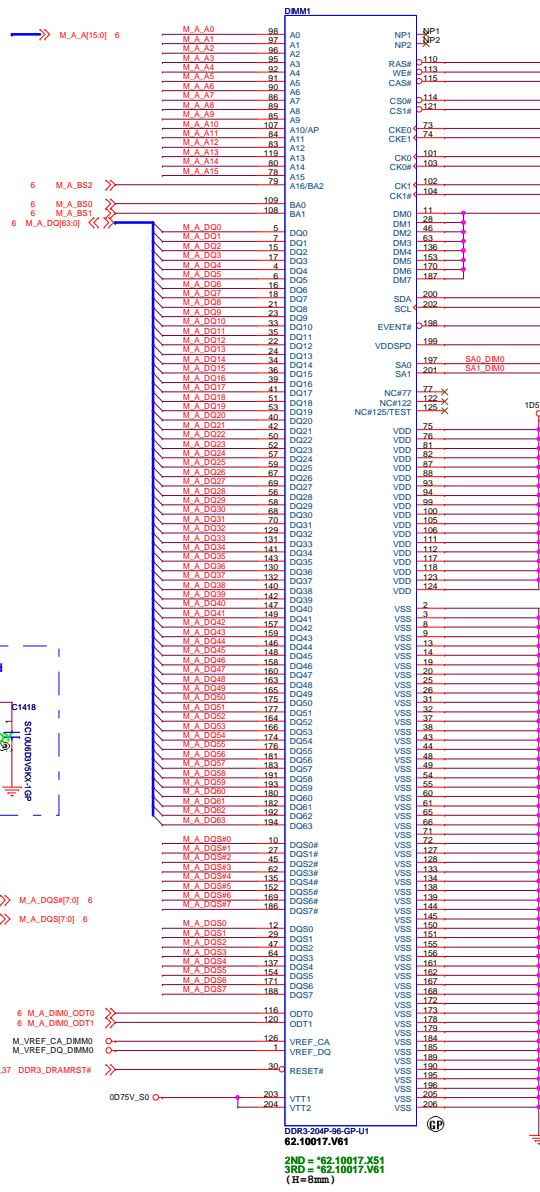
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Size A4	Document Number LA480		Rev SD
Date:	Friday, January 06, 2012		Sheet 13 of 103

SSID = MEMORY



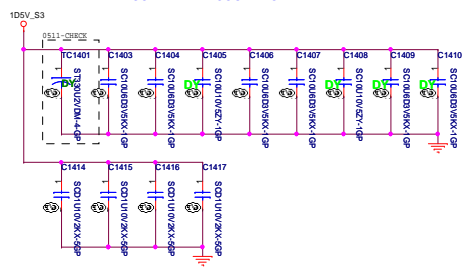
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Thermal EVENT



SODIMM A DECOUPLING



Layout Note:
Place these Caps near
SO-DIMMB.

SODIMM B DECOUPLING

The diagram illustrates the decoupling circuit for SODIMM B. It features a 125V_S3 power source connected to a series of capacitors (C1503-C1514) and inductors (L1503-L1514) arranged in two rows. The components are labeled with their values and footprints, and the layout includes ground connections and vias.

Top row components (left to right):

- C1503: 100nF, 0603, SMD
- L1503: 100nH, 0603, SMD
- C1504: 100nF, 0603, SMD
- L1504: 100nH, 0603, SMD
- C1505: 100nF, 0603, SMD
- L1505: 100nH, 0603, SMD
- C1506: 100nF, 0603, SMD
- L1506: 100nH, 0603, SMD
- C1507: 100nF, 0603, SMD
- L1507: 100nH, 0603, SMD
- C1508: 100nF, 0603, SMD
- L1508: 100nH, 0603, SMD
- C1509: 100nF, 0603, SMD
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- C1510: 100nF, 0603, SMD
- L1510: 100nH, 0603, SMD

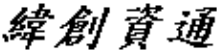
Bottom row components (left to right):

- C1511: 100nF, 0603, SMD
- L1511: 100nH, 0603, SMD
- C1512: 100nF, 0603, SMD
- L1512: 100nH, 0603, SMD
- C1513: 100nF, 0603, SMD
- L1513: 100nH, 0603, SMD
- C1514: 100nF, 0603, SMD
- L1514: 100nH, 0603, SMD

The layout includes ground connections and vias for the power and ground planes.

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DDR3-SODIMM2			
Size	Document Number		Rev
A4	LA480		SD
Date: Friday, January 06, 2012		Sheet 16	of 103

L_DDC_DATA(K47):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is
used for the local flat panel display

Close to PCH
 Close to PCH and keep 20mil
 away from other signal.

Close to PCH

Notes:
1K 0.5% 0402

The recommended value for this external resistor is 1.0 k $\pm 0.5\%$. The CRT DAC outputs may be measured when the display is completely white. If CRT DAC signal voltage value is between 665 mV to 770 mV, then the video level is within VESA specification and the reference resistor value is optimal for the motherboard design.

DDI Port B Detect: (SDVO_CTRL_DATA)
1: Port B detected
0: Port B not detected

HDMI

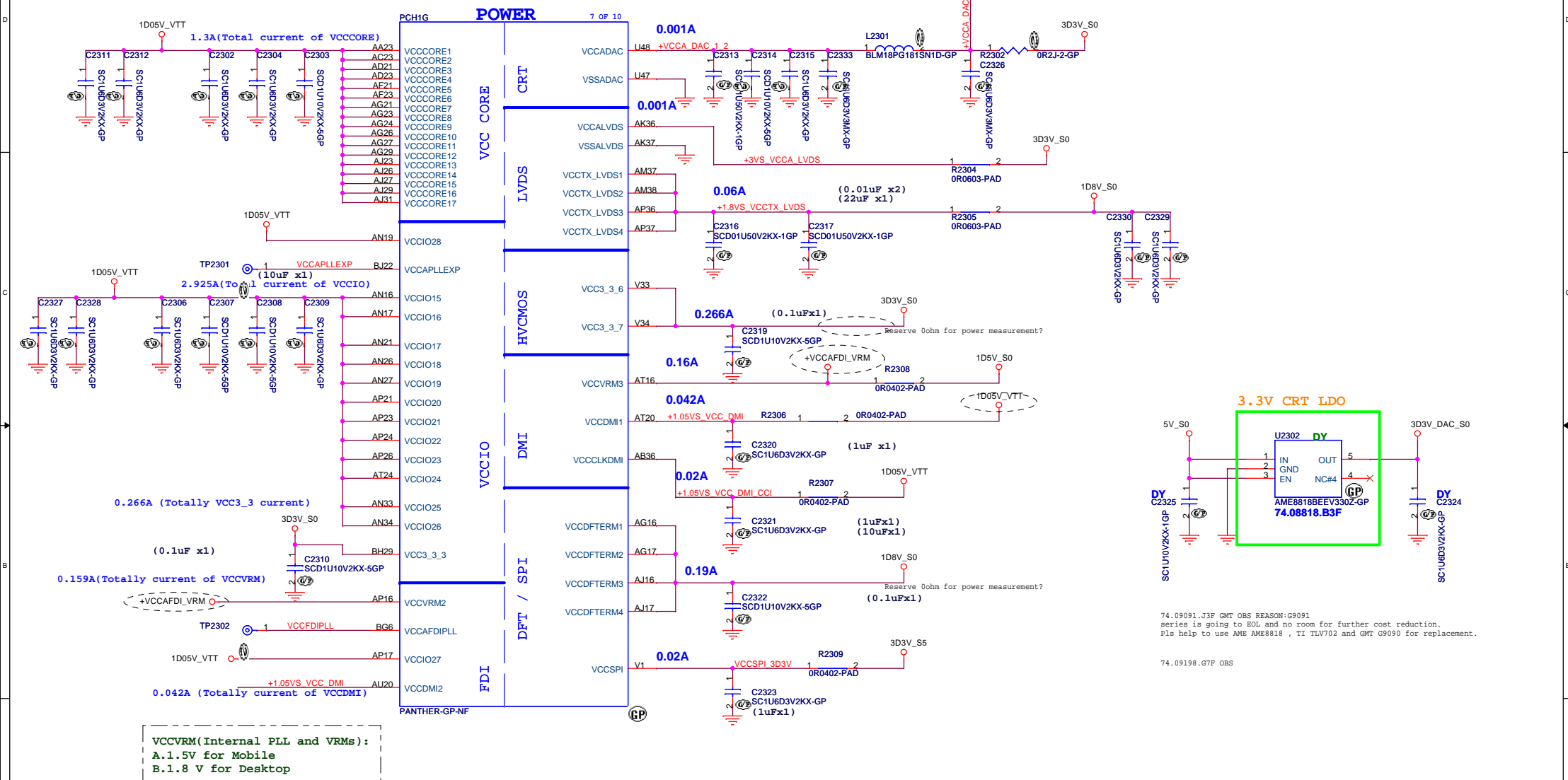
PORT	DDI PCH Pin Names	HDMI/DVI Mapping
PORT-B	DDPB_0[P]	TMDSB_DATA2#
	DDPB_0[N]	TMDSB_DATA2#
	DDPB_1[P]	TMDSB_DATA1#
	DDPB_1[N]	TMDSB_DATA1#
	DDPB_2[P]	TMDSB_DATA0#
	DDPB_2[N]	TMDSB_DATA0#
	DDPB_3[P]	TMDSB_CLK#
	DDPB_3[N]	TMDSB_CLK#
	DDPB_AUXN	NA
	DDPB_HPDP	HDMI_B_HPDP
	SDVO_CTRLCLK	HDMI_B_CTRLCLK
	SDVO_CTRLDATA	HDMI_B_CTRLDATA
	DDPC_0N	AY47
	DDPC_0P	AY49
	DDPC_1N	AY43
	DDPC_1P	AY45
	DDPC_2N	BA47
	DDPC_2P	BA49
	DDPC_3N	BB47
	DDPC_3P	BB49
	DDPD_CTRLCLK	M43
	DDPD_CTRLDATA	M36
	DDPD_AUXN	AT45
	DDPD_AUXP	AT43
	DDPD_HPDP	BH41
	DDPD_0N	BB43
	DDPD_0P	BB45
	DDPD_1N	BE43
	DDPD_1P	BE45
	DDPD_2N	BF43
	DDPD_2P	BF45
	DDPD_3N	BJ43
	DDPD_3P	BG43

<Core Design>

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Title		PCH : LVDS/CRT/DDI	
Size	Document Number	Rev	
A3	LA480	SD	
Date:	Friday, January 06, 2012	Sheet	17 of 103

6A



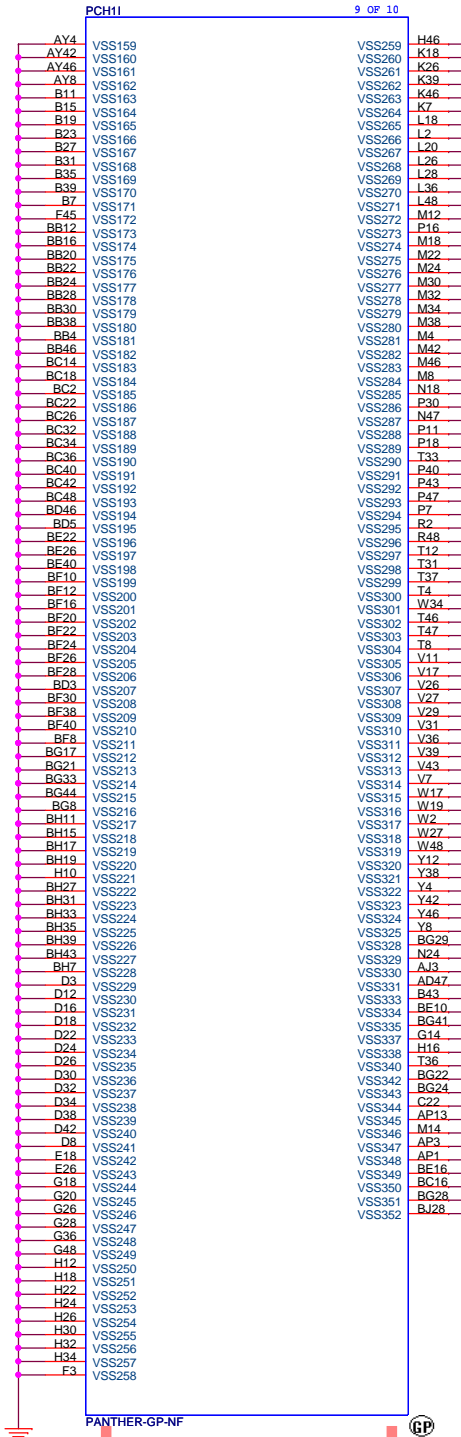
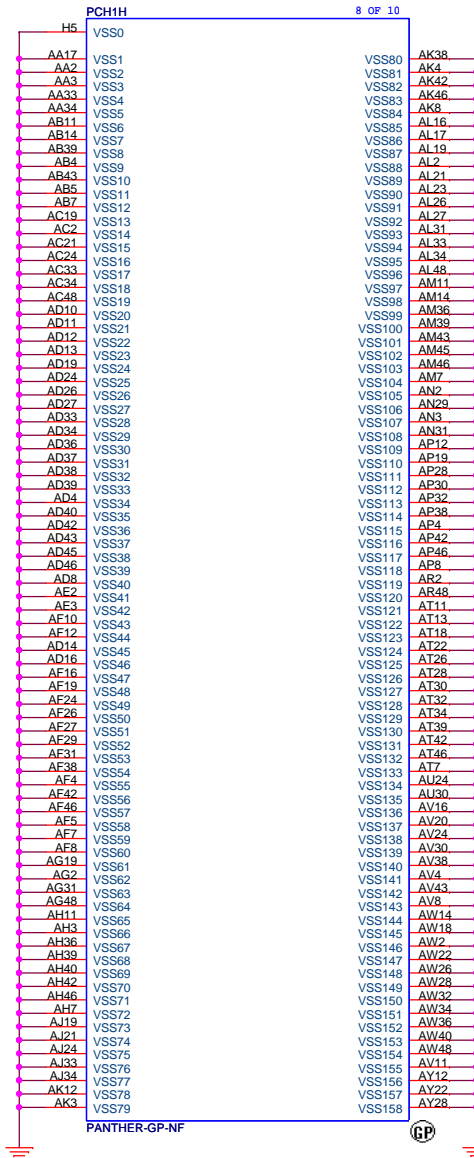
Refer to NPCE795 shared SPI flash architecture

<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH : POWER1		
Size	Document Number	Rev	
A3	LA480	SD	
Date:	Friday, January 06, 2012	Sheet	23 of 103

SSID = PCH



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		PCH : VSS	
Size	Document Number	Rev	SD
A3	LA480		
Date:	Friday, January 06, 2012	Sheet	25 of 103

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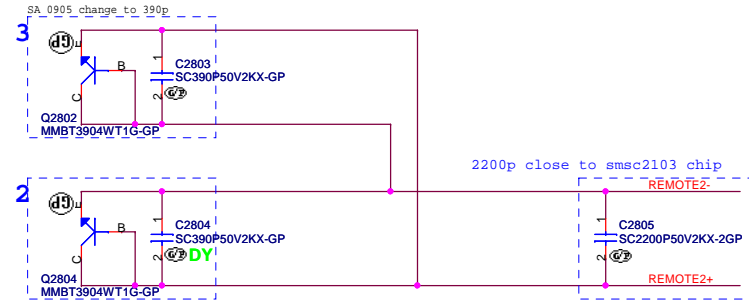
<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	LA480		SD
Date:	Friday, January 06, 2012		Sheet 26 of 103

SSID = Thermal

Thermal sensor

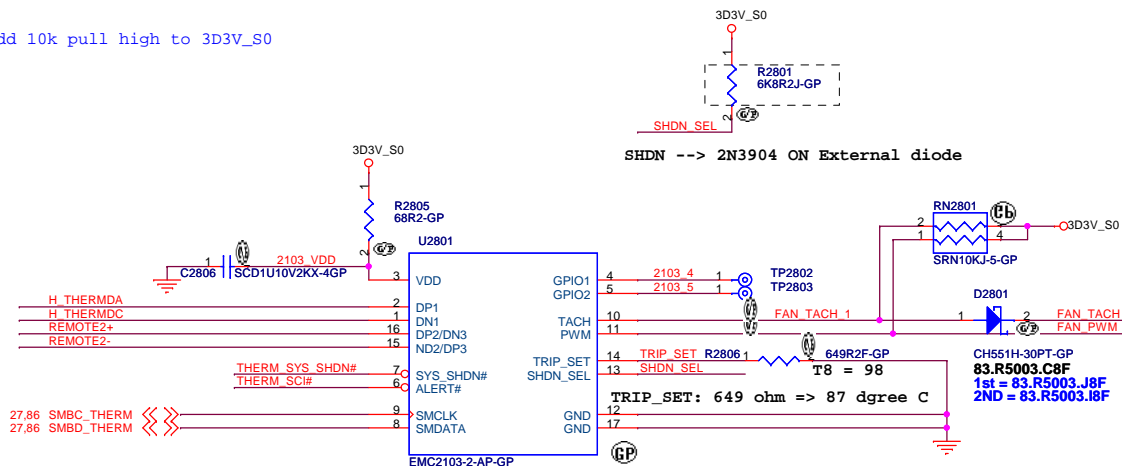
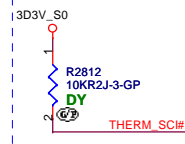
Close to SO-DIMM on top side.



between CPU, VGA and DIMM on bottom side

20110718_Carrey:

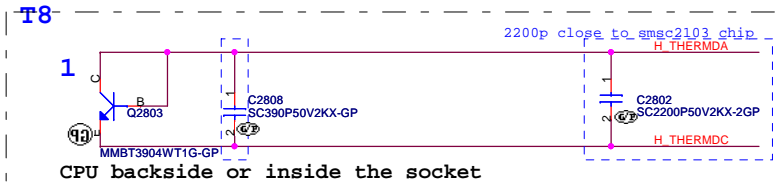
For Vendor suggestion, add 10k pull high to 3D3V_S0



pin6, ALERT# OD
pin7, SYS_SHDN# OD

20110718_Carrey:

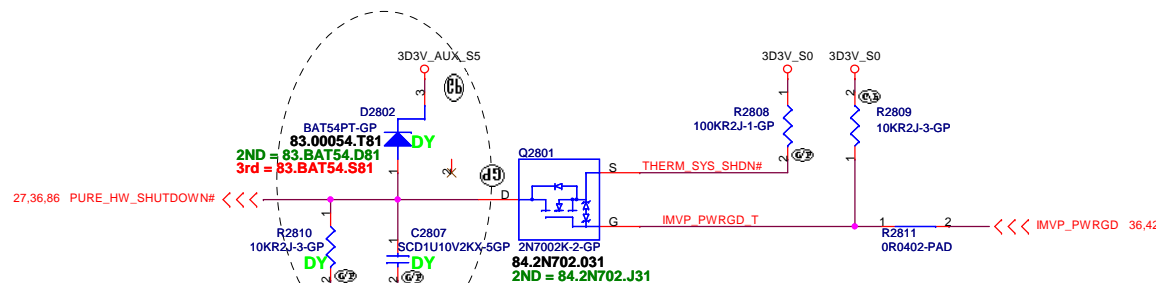
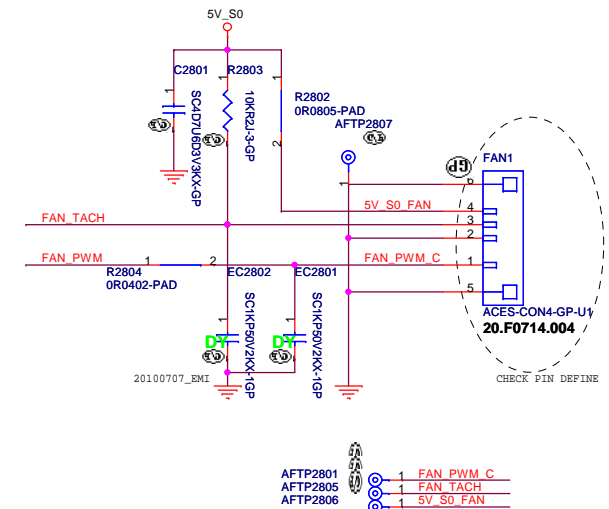
For Vendor suggestion, add 390pF Cap. as closed to pin B/C and E of Q2803



CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

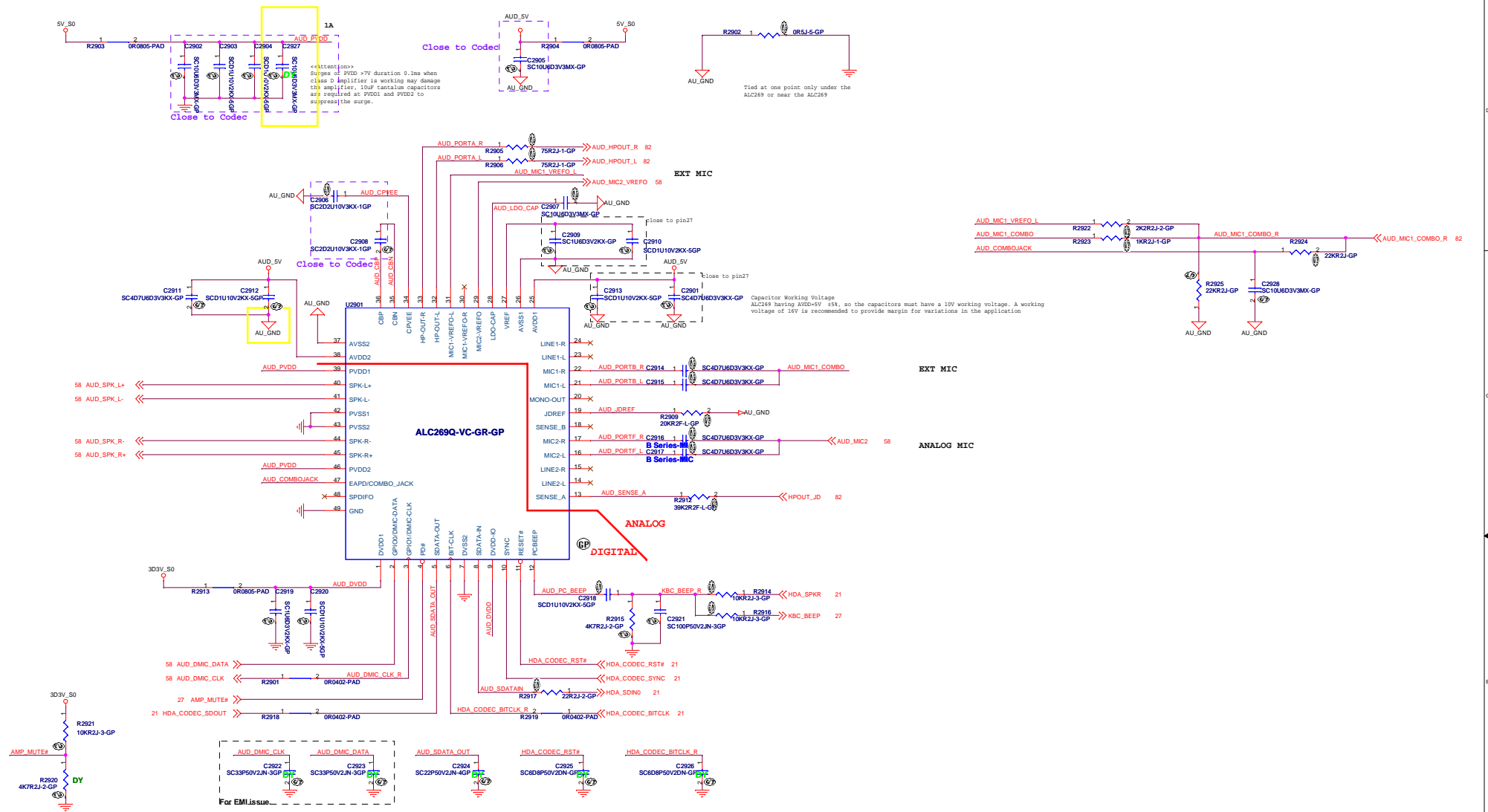
4 WIRE PWM Fan Control circuit



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
Size A3
Date: Friday, January 06, 2012
Document Number
LA480
Sheet 28 of 103
SD



<Core Design>

緯創資通 Wistron Corporation
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichang,
Taipei Hsien 221, Taiwan, R.O.C.

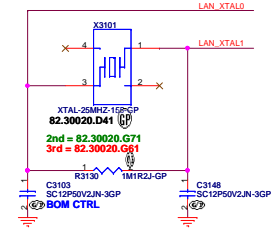
AUDIO CODEC			
File	Document Number	Rev	SD
Size	LA480		
AC			
Date	Friday, January 06, 2012	Sheet 26 of 103	

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<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	LA480		SD
Date: Friday, January 06, 2012		Sheet 30 of	103

25MHz XTAL

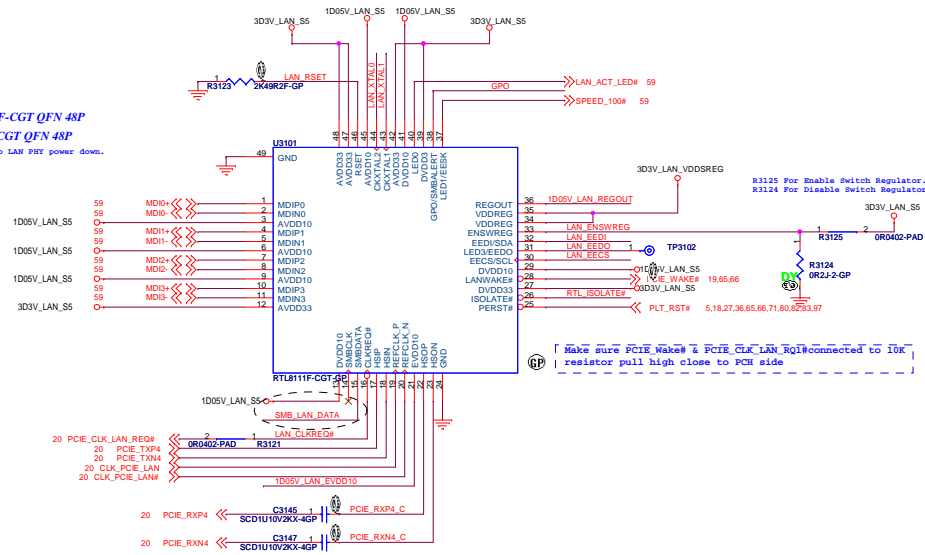


	C3103	C3148
VB480	15pF 78.15034.1FL	12pF
VB580	12pF 78.12034.1FL	12pF

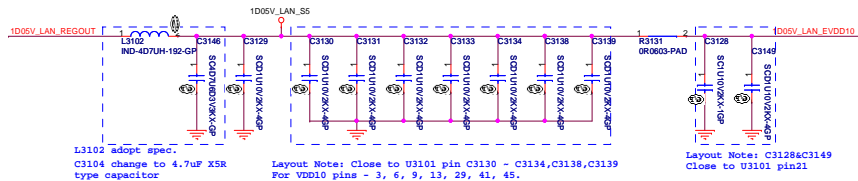
71.08111.N03, IC PCIE CTRL RTL8111F-CGT QFN 48P

71.08111.J03, IC PCIE RTL8111E-VL-CGT QFN 48P

8111F can use GPIO to inform system to do LAN PHY power down.

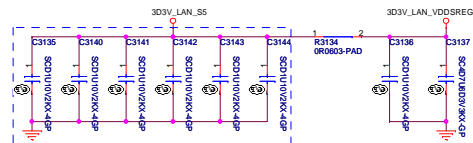


Make sure PCIE_Wake# & PCIE_CLK_LAN_Rst# connected to 10K resistor pull high close to PCN side

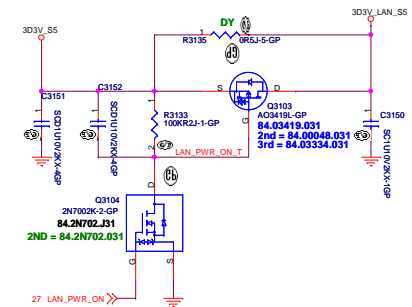
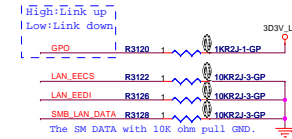
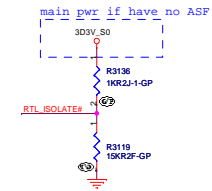


Layout Note: Close to U3101 pin C3130 - C3134, C3138, C3139 For VDD10 pins - 3, 6, 9, 13, 29, 41, 45.

Layout Note: C3128&C3149 Close to U3101 pin21



Layout Note: C3135, C3140-C3144 Close to U3101 pin For VDD33 pins - 12, 27, 39, 42, 47, 48.



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LAN RTL8111F			
File	Document Number	Rev	SD
LA480			
Friday, January 06, 2012	Sheet 31 of 103		

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<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

Document Number

LA480

Rev

SD

Date: Friday, January 06, 2012

Sheet 33 of 103

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<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	LA480		SD
Date:	Friday, January 06, 2012		Sheet 34 of 103

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<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB 3.0 Controller

Size

A4

Document Number

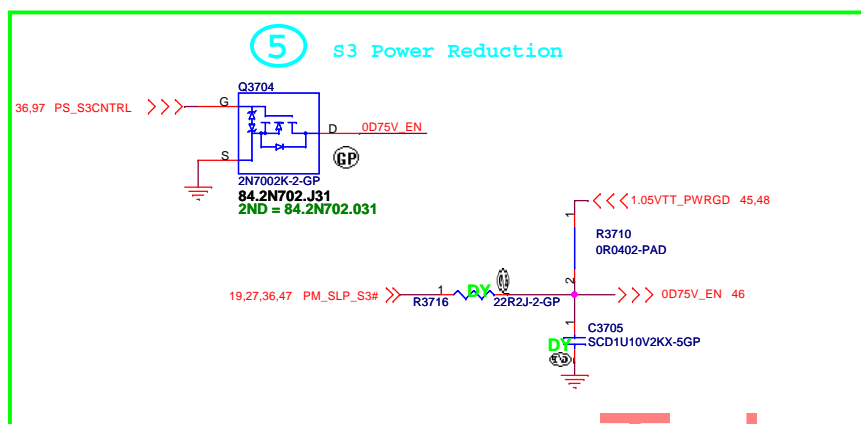
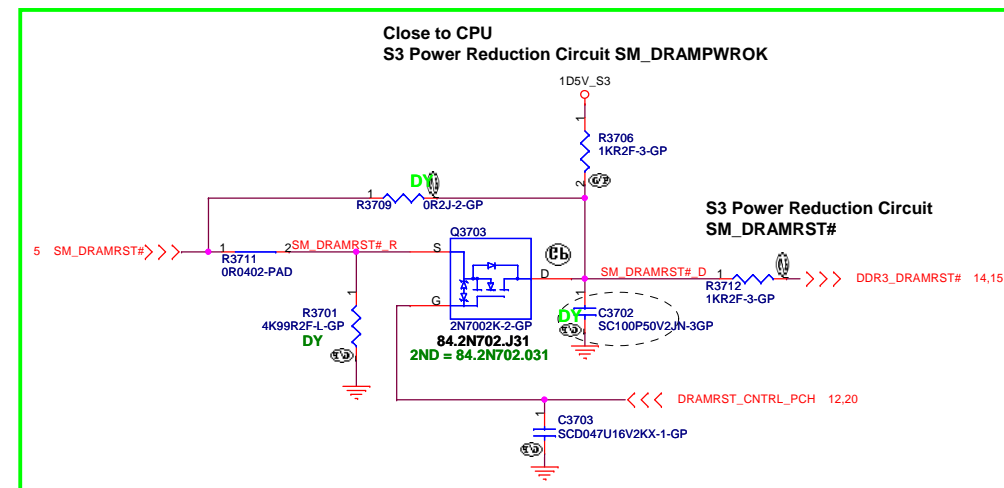
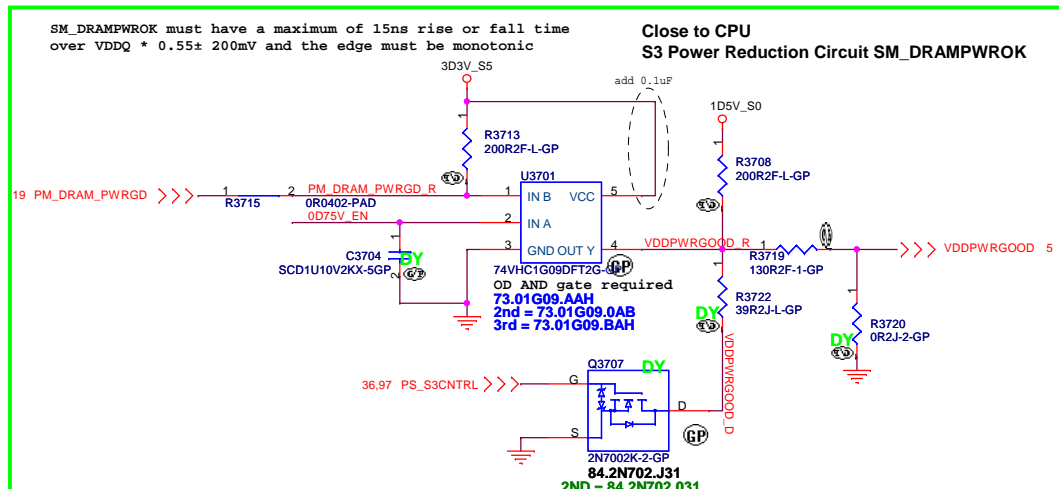
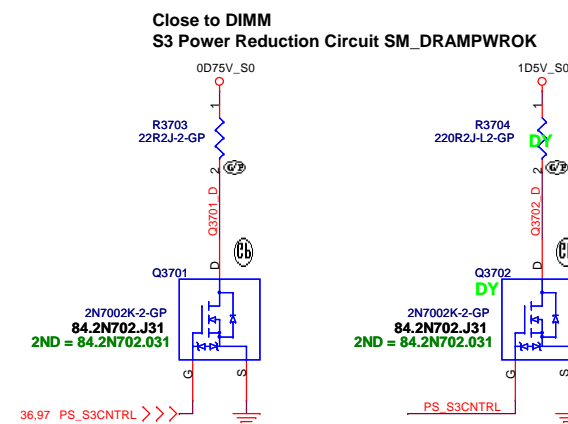
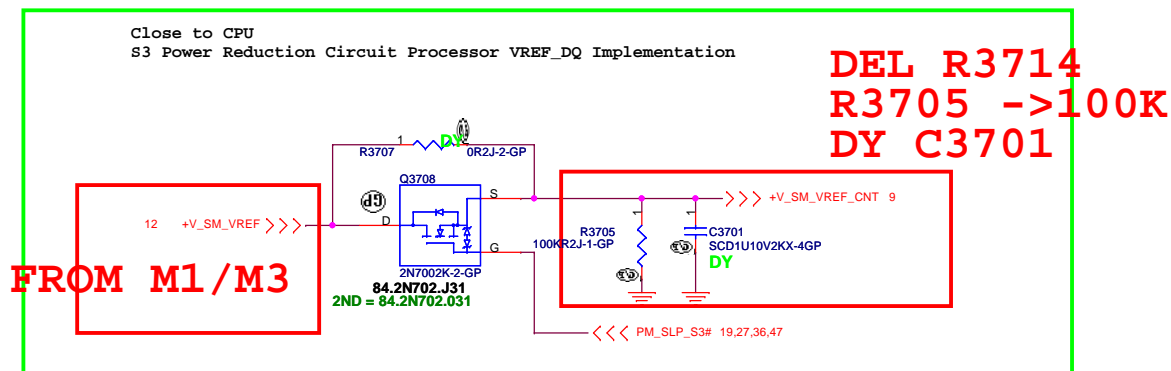
LA480

Rev

SD

Date: Friday, January 06, 2012

Sheet 35 of 103

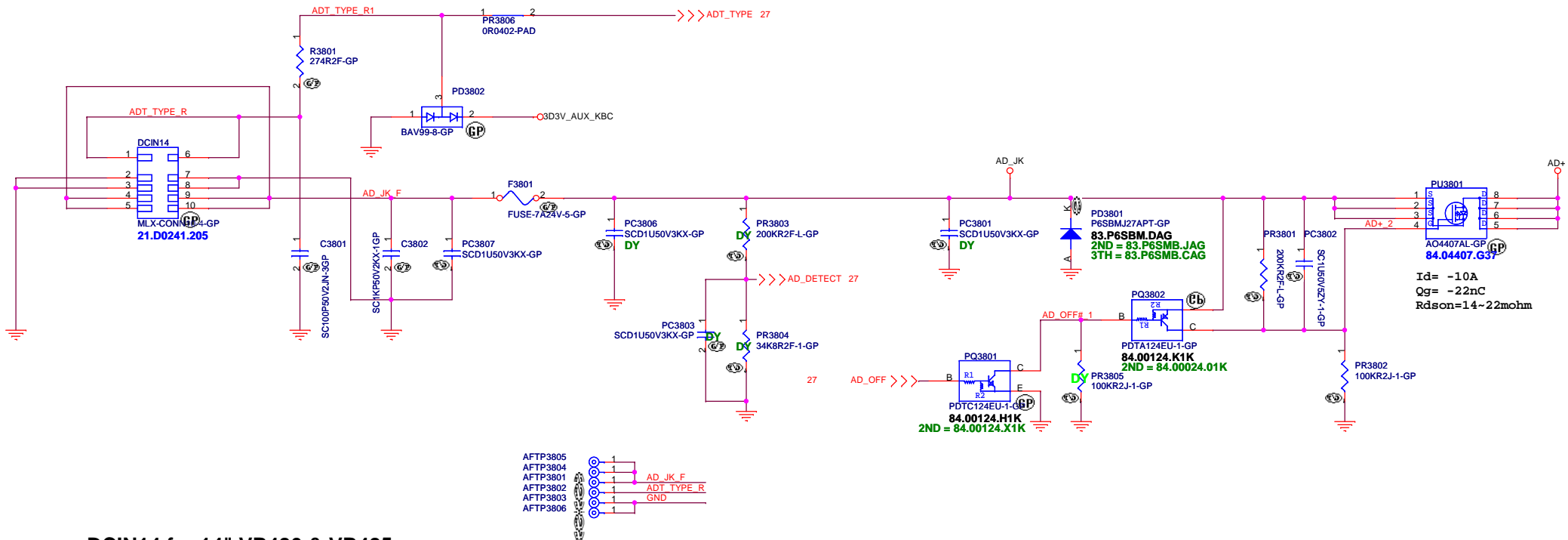


<Core Design>

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Title ADAPTER
Size A3 Document Number LA480
Date: Friday, January 06, 2012 Sheet 37 of 103
Rev SD

Adaptor in to generate DCBATOUT

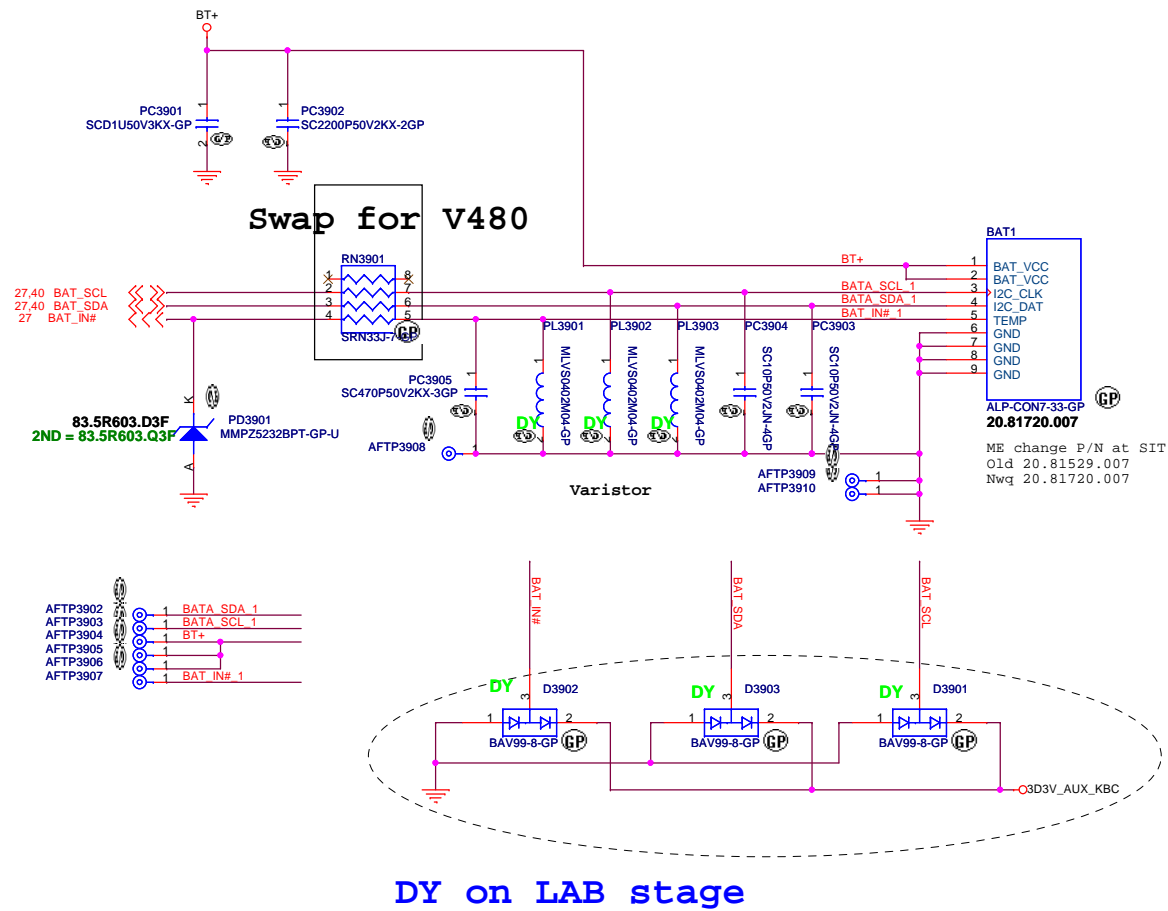


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		DCIN_JACK	
Size	Document Number	LA480	Rev
A3			SD
Date:	Friday, January 06, 2012	Sheet 38 of 103	

BATTERY CONNECTOR



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		BATT_CONN	
Size	Document Number	LA480	Rev
Date: Friday, January 06, 2012			SD
Sheet	39	of	103

SSID = Charger

A8(ANNIE/ASTRO)
PR4007,PR4008

AD+ total power	R1	R2
65w	64.12425.6DL	100K
80w	41.2k	100K
90w	60.4k	100K
120w	64.40425.6DL	100K

STOP_CHG#
connects to KBC

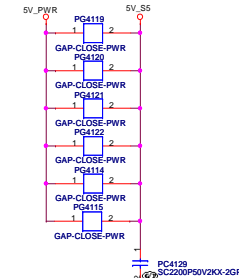
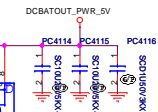
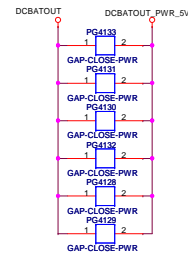
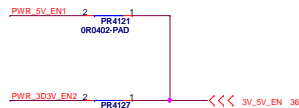
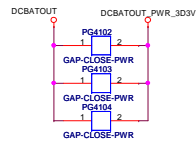
Charger Current=1.4~3.6A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1 Main Tai Wu Rd, Hsinchu,
Taipei Hsien 301, Taiwan, R.O.C

File	<Title>	Rev
Size	Document Number	SD
A2	LA480	
Date:	Friday, January 06, 2012	Sheet 40 of 103

SSID = PWR.Plane.Regulator_5v3p3v



Design Current=5.25A
OCP>7.8A

Cyntec. 2.2uH 7.3*6.3
DCR=18~20mohm
Idc=8A, Isat=14A

Id=12A, Qg=3.8nC,
Rds(on)=24~30 mohm

Id=12A, Qg=3.8nC,
Rds(on)=24~30 mohm

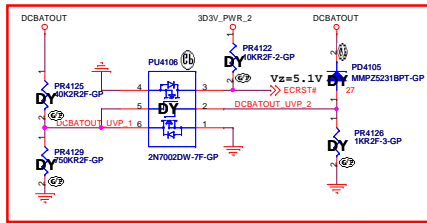
Design Current=5.25A
OCP>7.8A

Cyntec. 3.3uH 6.5*6.9*3
DCR=28~30mohm
Idc=6A, Isat=13.5A

Id=16A, Qg=7.3nC,
Rds(on)=13.5~16.5 mohm

Close to VFB Pin (pin2)

Close to VFB Pin (pin5)



<Core Design>

緯創資通 Wistron Corporation
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TPS51123_5V_3D3V		
Size	Document Number	Rev
Date	Friday, January 08, 2012	Sheet 41 of 104

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	Main source	2nd source
PU4301	84.03606.037 FDMS3606S-GP-U	
PU4302	84.03606.037 FDMS3606S-GP-U	
PU4303	84.03606.037 FDMS3606S-GP-U	
PU4304	84.03606.037 FDMS3606S-GP-U	

BOM control

Design current: 42.4A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title TPS51640_CPU_CORE(2/3)

Size Document Number

<Doc>

Rev

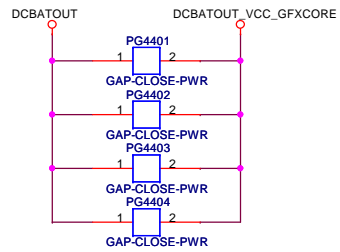
SD

Date: Friday, January 06, 2012

Sheet 43 of 103

	Main source	2nd source
PU4402	84.07608.037 FDMS7608S-GP	
PU4403	84.07608.037 FDMS7608S-GP	

BOM control

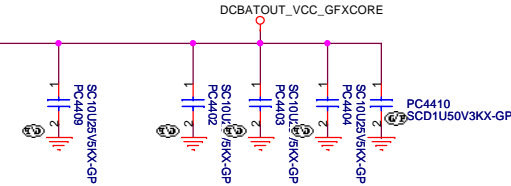
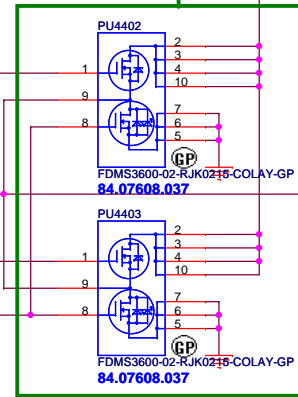
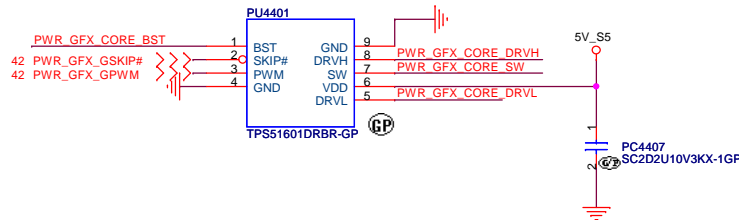


PWR_GFX_CORE_DRVH

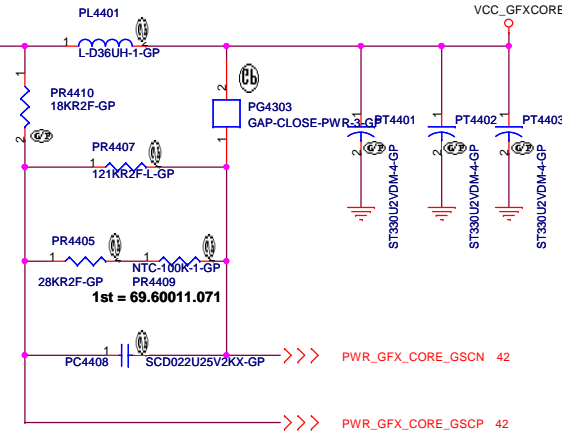
PWR_GFX_CORE_SW

PWR_GFX_CORE_BST

PWR_GFX_CORE_DRVL



Design current: 22A



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title TPS51640_CPU_CORE(3/3)

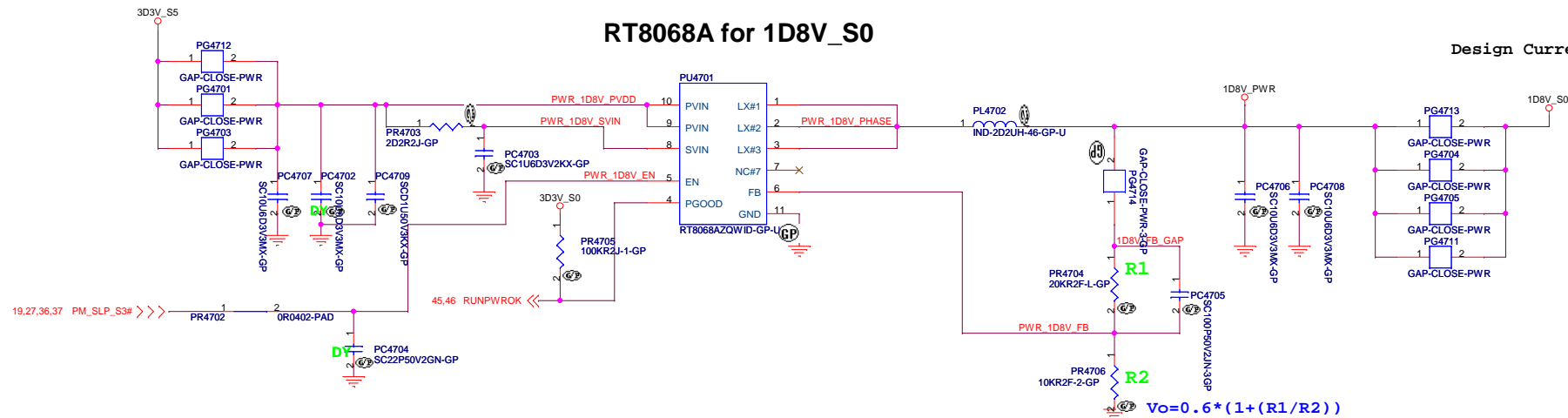
Size Document Number <Doc> Rev SD

Date: Friday, January 06, 2012 Sheet 44 of 103

SSID = PWR.Plane.Regulator_1p8v

RT8068A for 1D8V_S0

Design Current=1.1A

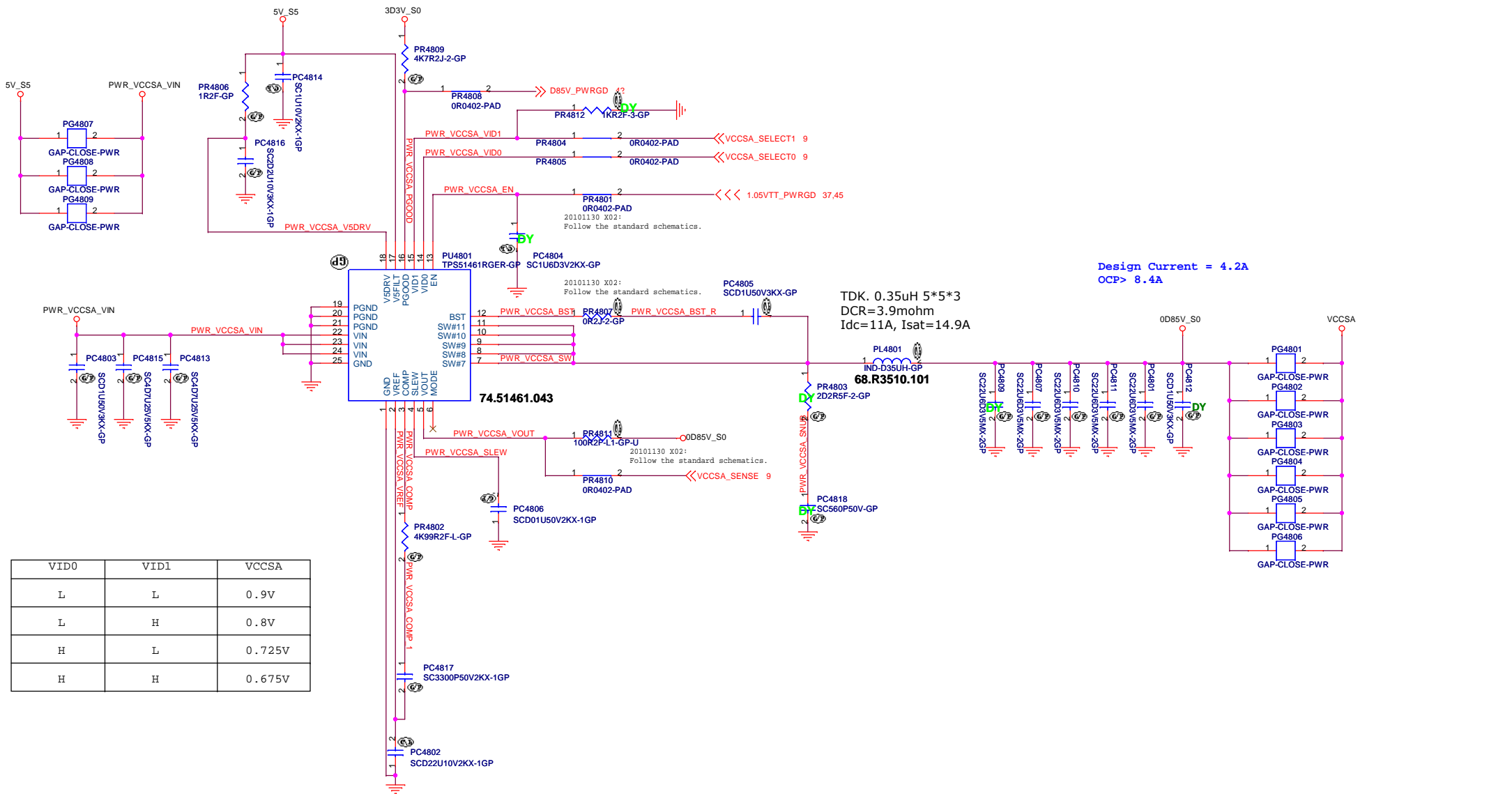


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		Rev
PWM_1D8V_RT8015B		SD
Size	Document Number	Rev
Date: Friday, January 06, 2012	Sheet 47 of 103	

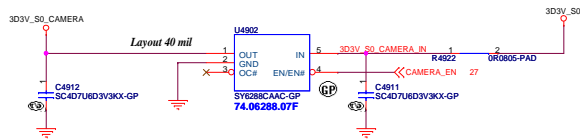
TPS51461 for VCCSA



LCD / Inverter Connector

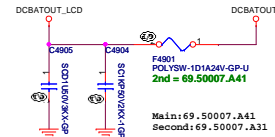


CAMERA POWER

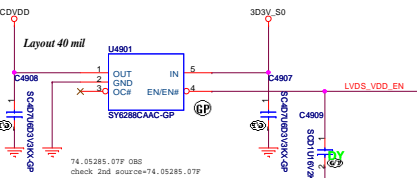
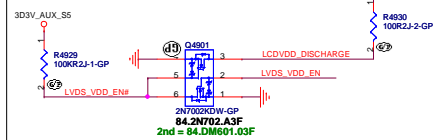


SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active

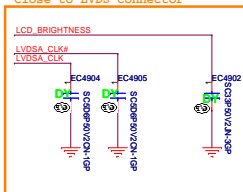
LCD POWER



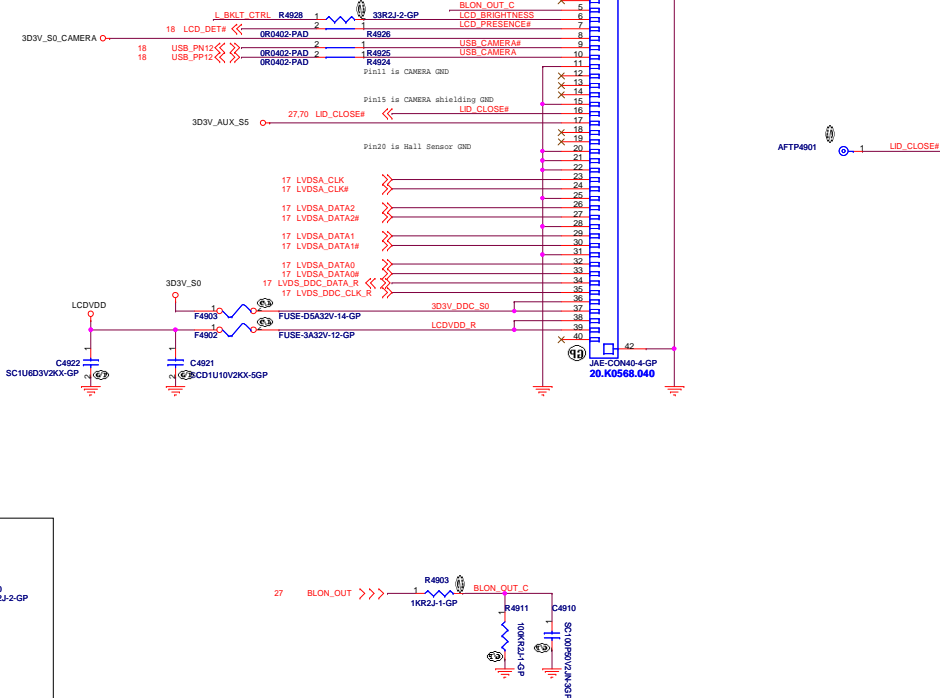
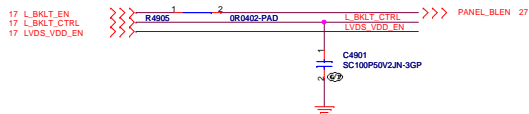
LCDVDD Discharge



For EMI request
Close to LVDS connector



Panel BL brightness/Power En/BL En

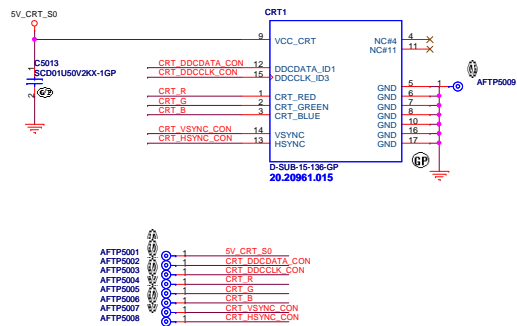


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsiao Tai Wu Rd., Hsuehshih,
Taichung Hsien 421, Taiwan, R.O.C.

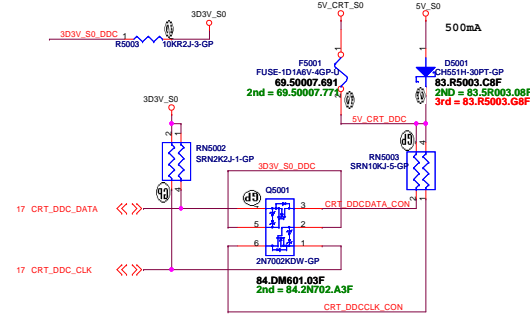
File	Document Number	Rev
A2	LCD Connector	SD
Date	Friday, January 06, 2012	Sheet 48 of 103

CRT connector

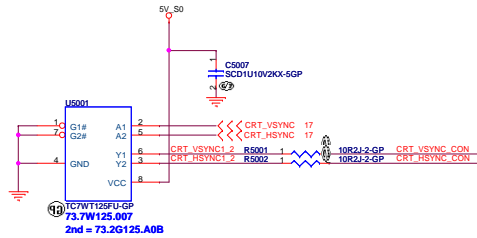


CRT DDCDATA & DDCCLK level shift

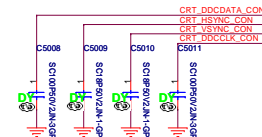
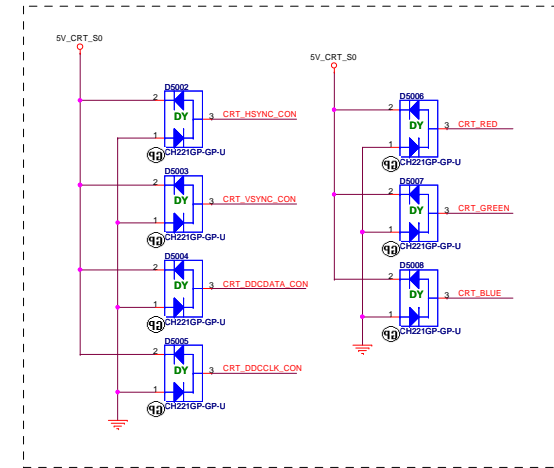
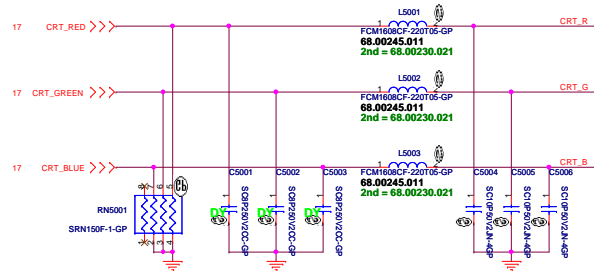
Pull High 5V Design on CRT Board



CRT Hsync & Vsync level shift

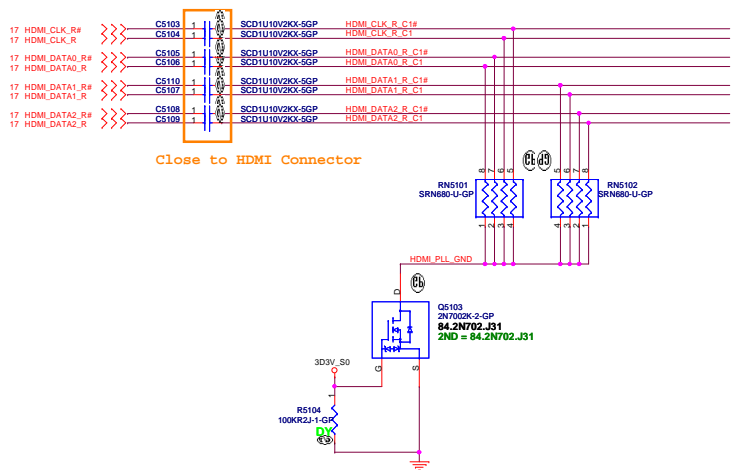


CRT RGB

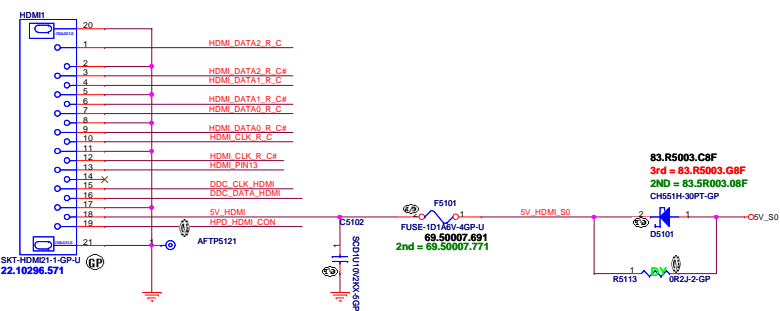


HDMI Passive Level Shifter

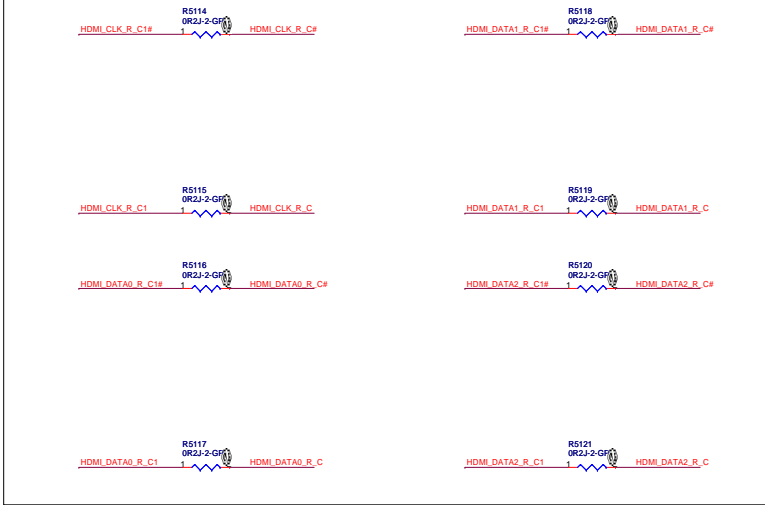
Close to HDMI Connector



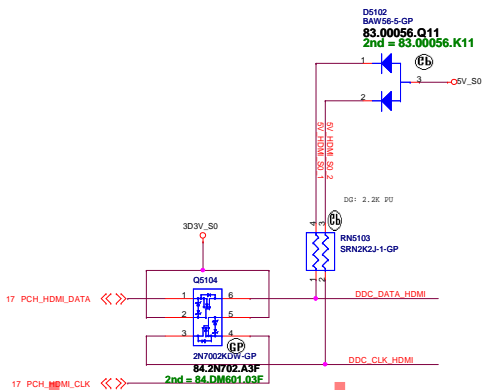
HDMI CONNECTOR



EMI's request



HDMI DDC Passive Level Shifter



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<Core Design>

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Title

eDP

Size

A4

Document Number

LA480

Rev

SD

Date: Friday, January 06, 2012

Sheet 52 of 103

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<Core Design>

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

S-VIDEO

Size

A4

Document Number

LA480

Rev

SD

Date: Friday, January 06, 2012

Sheet 53 of 103

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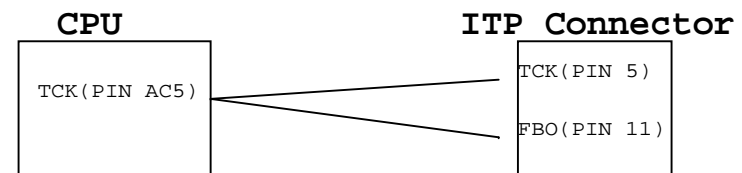
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	LA480		SD
Date: Friday, January 06, 2012		Sheet 54 of	103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



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Title

ITP

Size

A4

Document Number

LA480

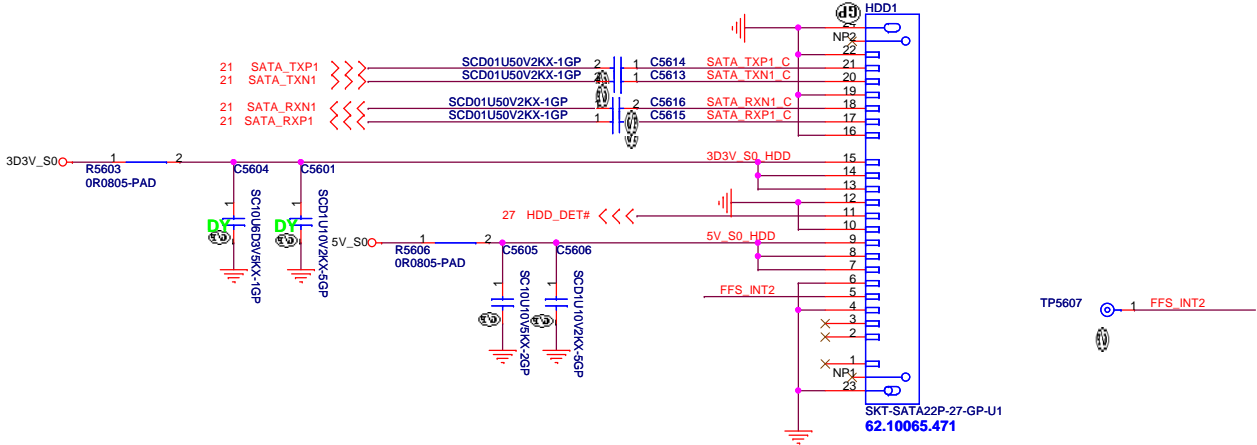
Rev

SD

Date: Friday, January 06, 2012

Sheet 55 of 103

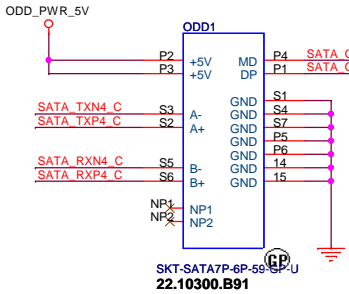
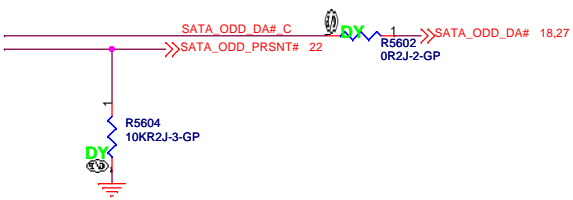
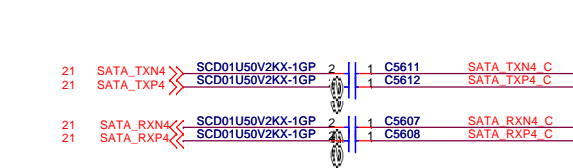
SATA HDD Connector



ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.

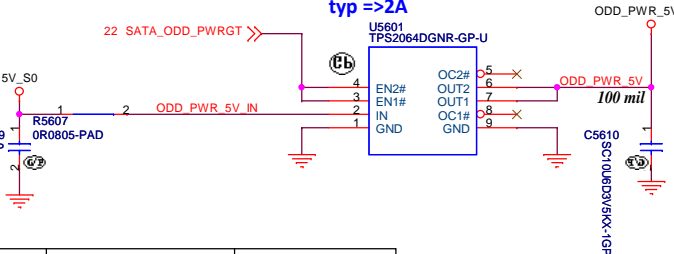


When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

- 74.02069.079 TI TPS2069DGNR MSOP 8P
- 74.07534.D79 UPI UF7534PRA8-15 MSOP 8P
- 74.00547.C79 GMT G547F1P81U MSOP 8P (OBS)
- 74.07534.A79 UPI UF7534ARA8-15 MSOP8P

SATA Zero Power ODD

Current limit
Active High
typ =>2A



TI	74.02069.079	TPS2069DGNR	High Active
DIODES		AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active

SUPPORT ZERO SATA ODD

<Core Design>

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File

Size

A3

Document Number

LA480

Rev

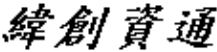
SD

Date: Friday, January 06, 2012

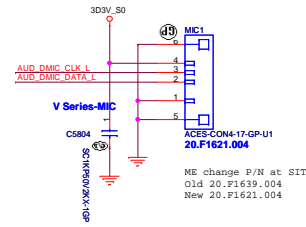
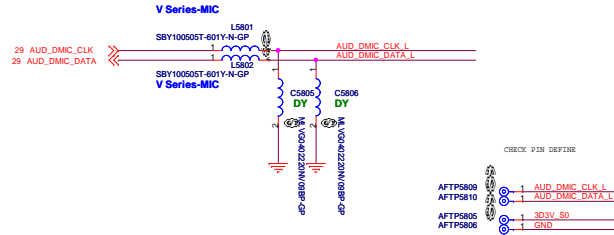
Sheet 56 of 103

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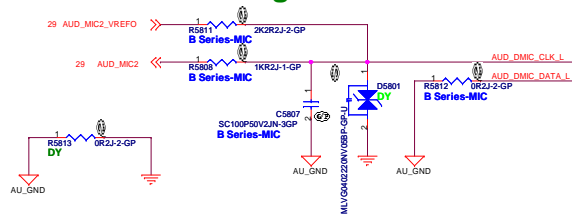
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
E-SATA+USB			
Size	Document Number		Rev
A4	LA480		SD
Date:	Friday, January 06, 2012		Sheet 57 of 103

Int. Digital MIC for V series



Int. Mono Analog MIC for B series



INTERNAL STEREO SPEAKERS

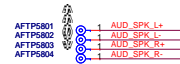
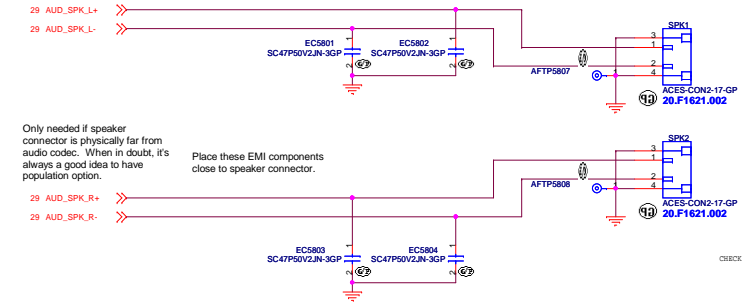


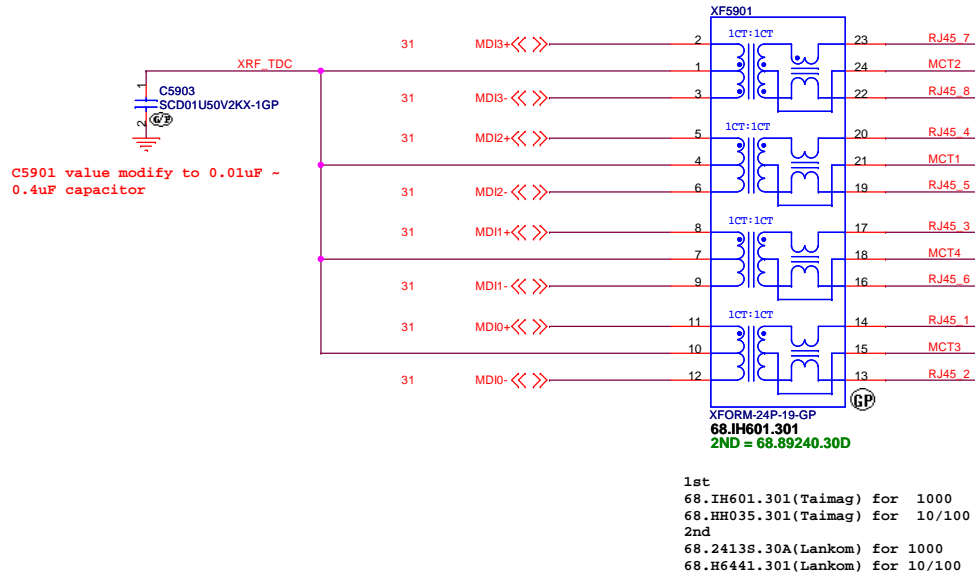
Table 58.1 - Bi-direction ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	RSB5.6SMT2R	N/A	83.RSB56.BAF
ON SEMI	ESD5B5.0ST1G	N/A	83.ESD5B.0AF
NXP	PESD5V0S1BB	N/A	83.0005V.0AF

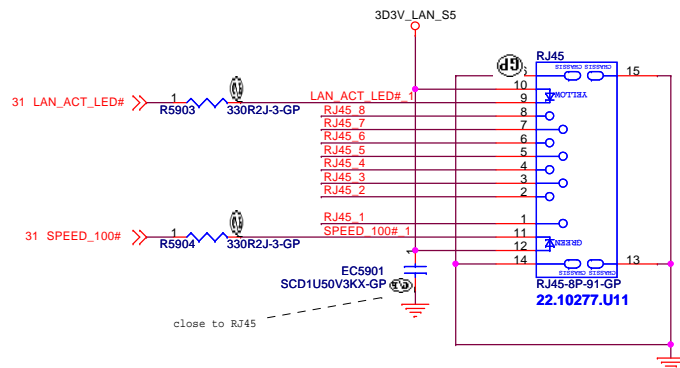
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FOR CO-LAY

GIGA Lan Transformer



LAN Connector



TVS

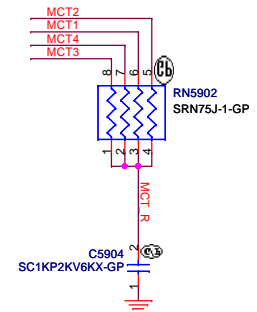
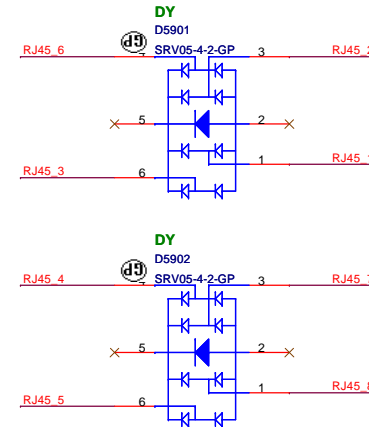
83.00005.BAE

DIODE ARR SRV05-4.TCT SOT-23-6

83.09904.AAE

DIODE ESD AZC099-04S SOT23-6L

Swap for V480



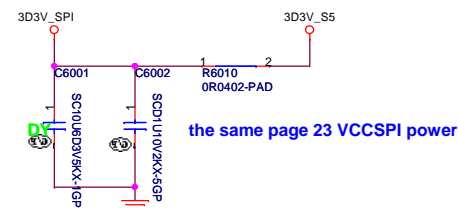
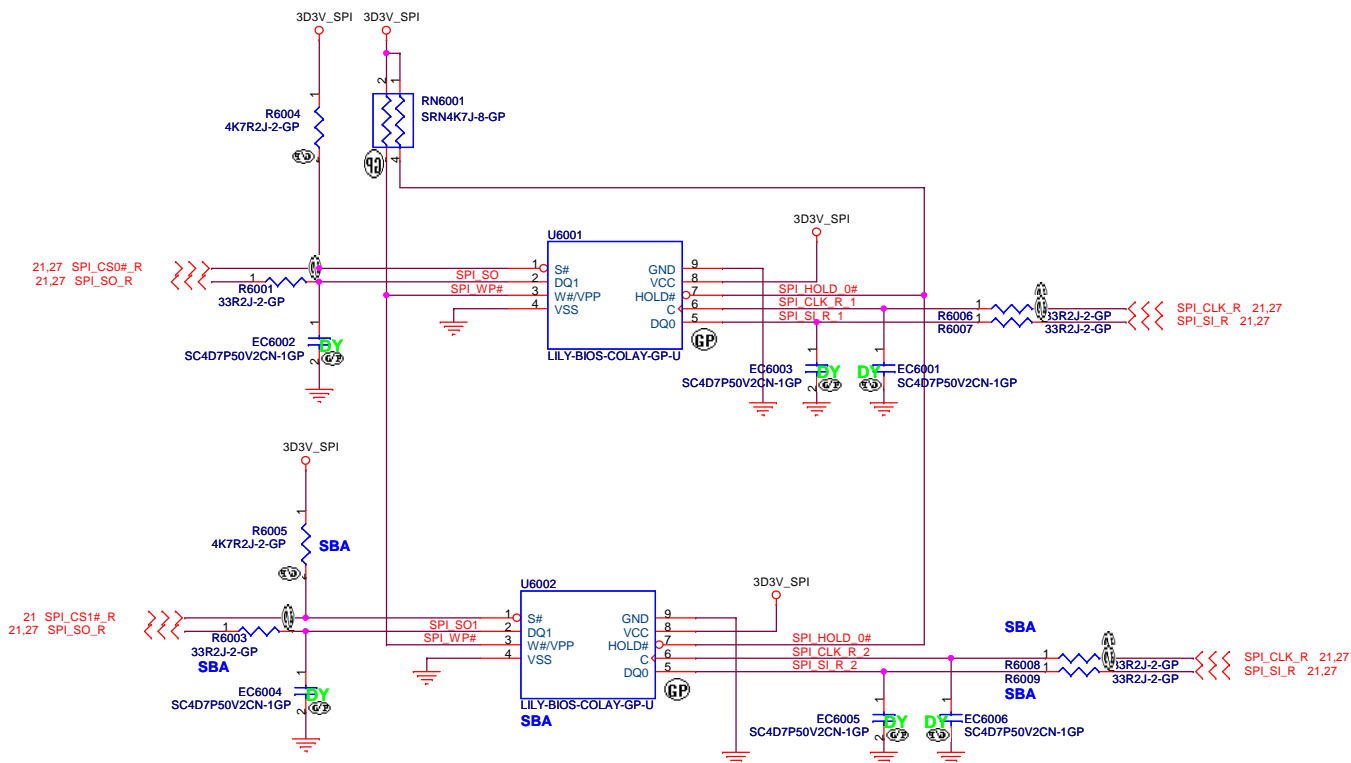
<Core Design>

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Title			
RJ45 / Transformer			
Size	Document Number		Rev
A3	LA480		SD
Date:	Friday, January 06, 2012	Sheet 59 of 103	

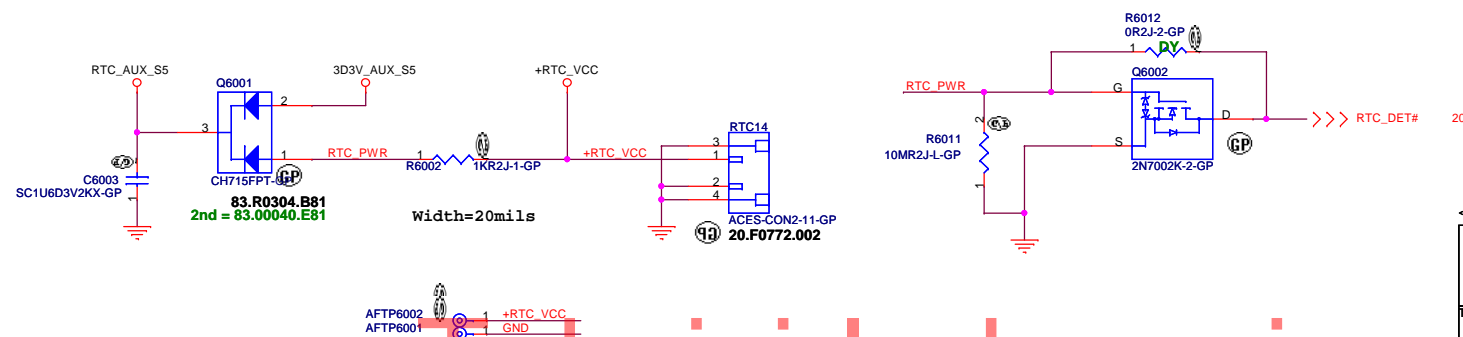
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH



4MB			
SO8	Marconix	MX25L3206EM2I-12G	72.25320.C01
	Winbond	W25Q032BVSSIG	72.25Q32.A01
	Numonyx	N25Q032A13ESE40	72.25032.H01
8MB			
SO8	Marconix	MX25L6406EM2I-12G	72.25640.D01
	Winbond	W25Q064CVSSIG	72.25Q64.B01
	Numonyx	N25Q064A13ESE40	72.25Q64.D01
16MB			
WSON	Marconix	MX25L12836EZNI-10G	72.25128.X01
	Marconix	MX25L12835EZNI-10G	72.25128.Y01
	Winbond	W25Q128BVEIG	72.25128.I01
	Numonyx	N25Q128A13EF840	72.25128.B03

SSID = RBATT

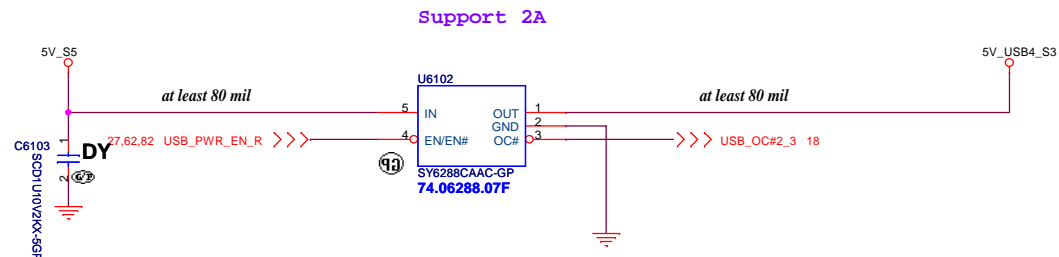


<Core Design>

緯創資通 Wistron Corporation
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Title		Flash/RTC
Size	Document Number	Rev
A3	LA480	SD
Date:	Friday, January 06, 2012	Sheet 60 of 103

USB Board CONN.



Place U6102 close to USBCN1

<Core Design>

緯創資通

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Title

USB Connector

Size

A3

Document Number

LA480

Rev

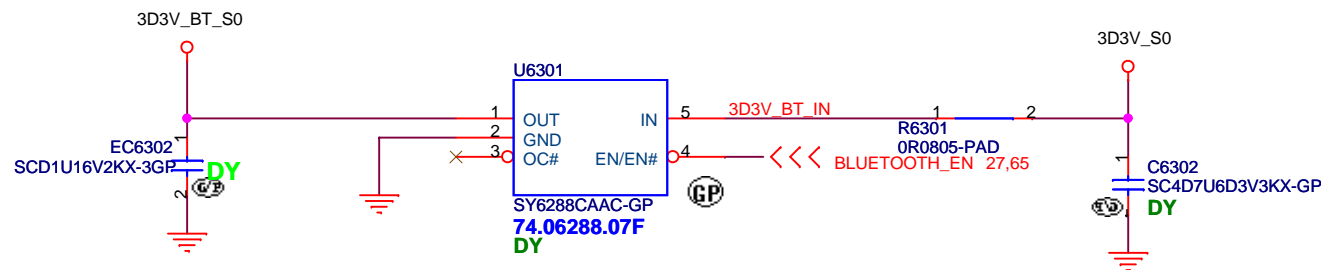
SD

Date: Friday, January 06, 2012

Sheet 61 of 103

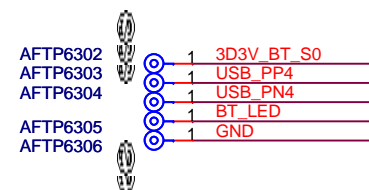
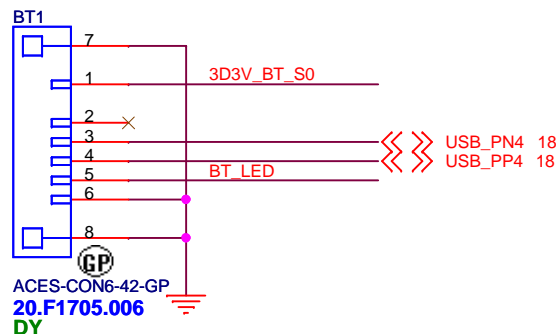
SSID = User.Interface

Bluetooth conn.



BT Module pin definition is same as LA470

SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Bluetooth

Size A4 Document Number

LA480

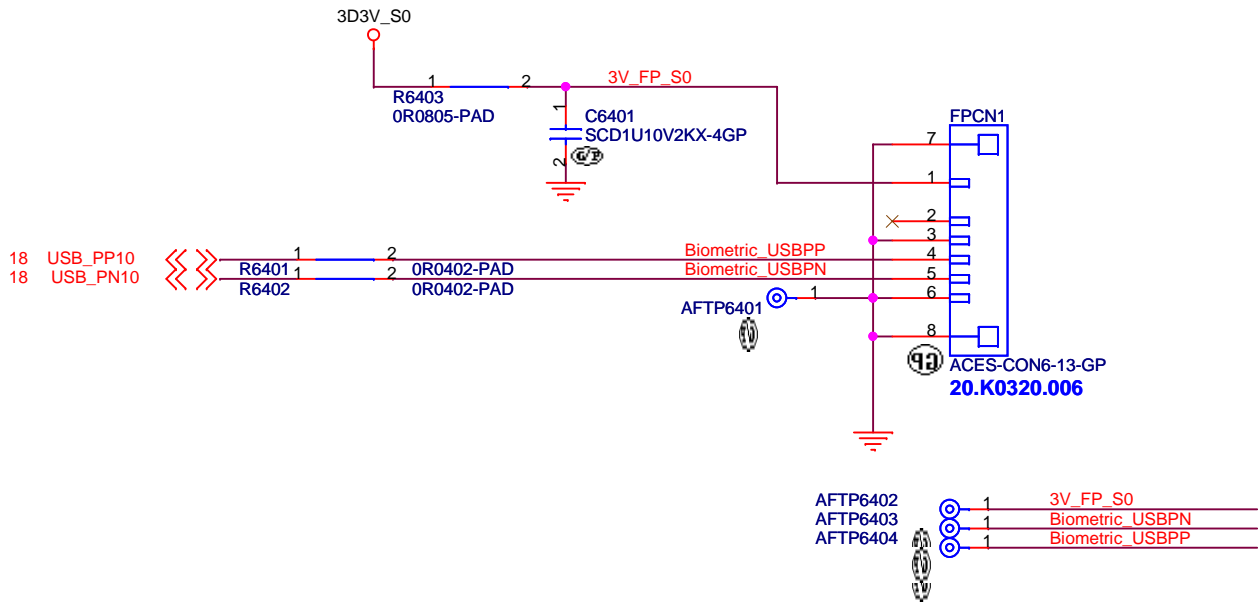
Rev

SD

Date: Friday, January 06, 2012

Sheet 63 of 103

Finger Printer Connector

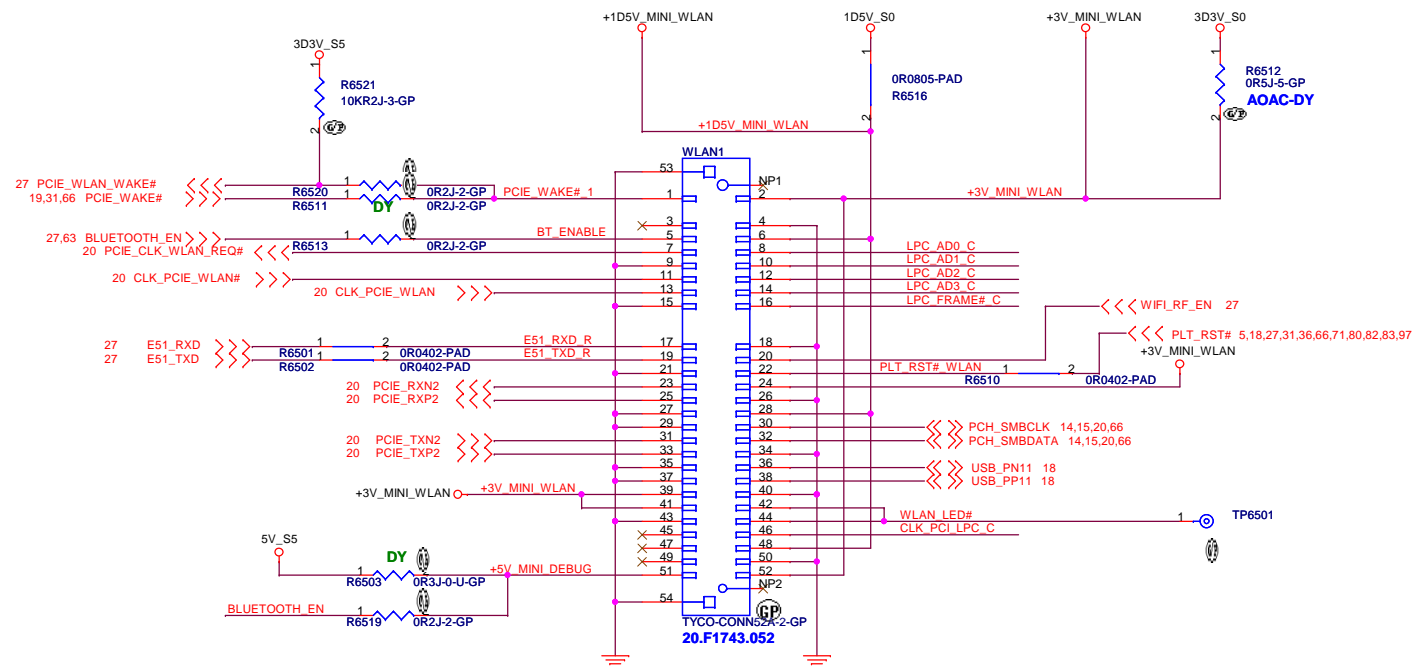


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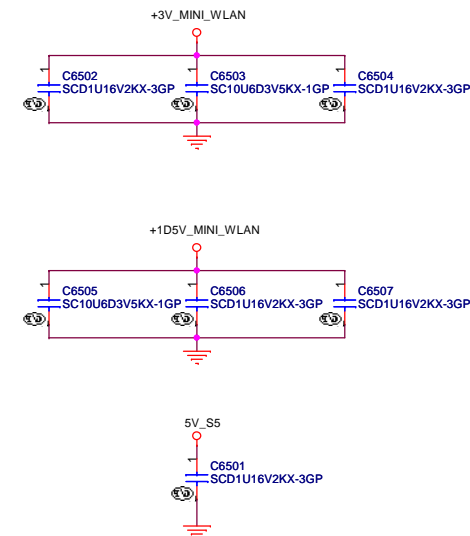
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Finger Printer Connector			
Size	Document Number		Rev
A4	LA480		SD
Date:	Friday, January 06, 2012	Sheet	64 of 103

SSID = Wireless

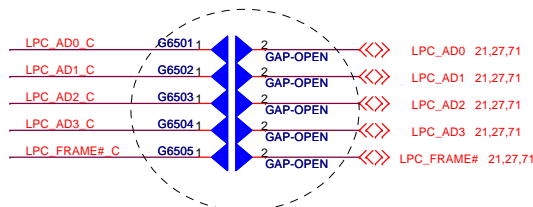
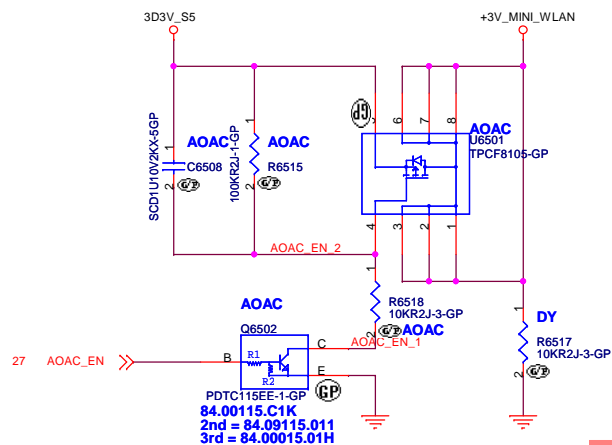
Mini Card Connector(802.11a/b/g/n)



Place near MINI Card CONN



Reserve for AOAC



G6506~G6511
placement close close WLAN1
in bottom side

<Core Design>

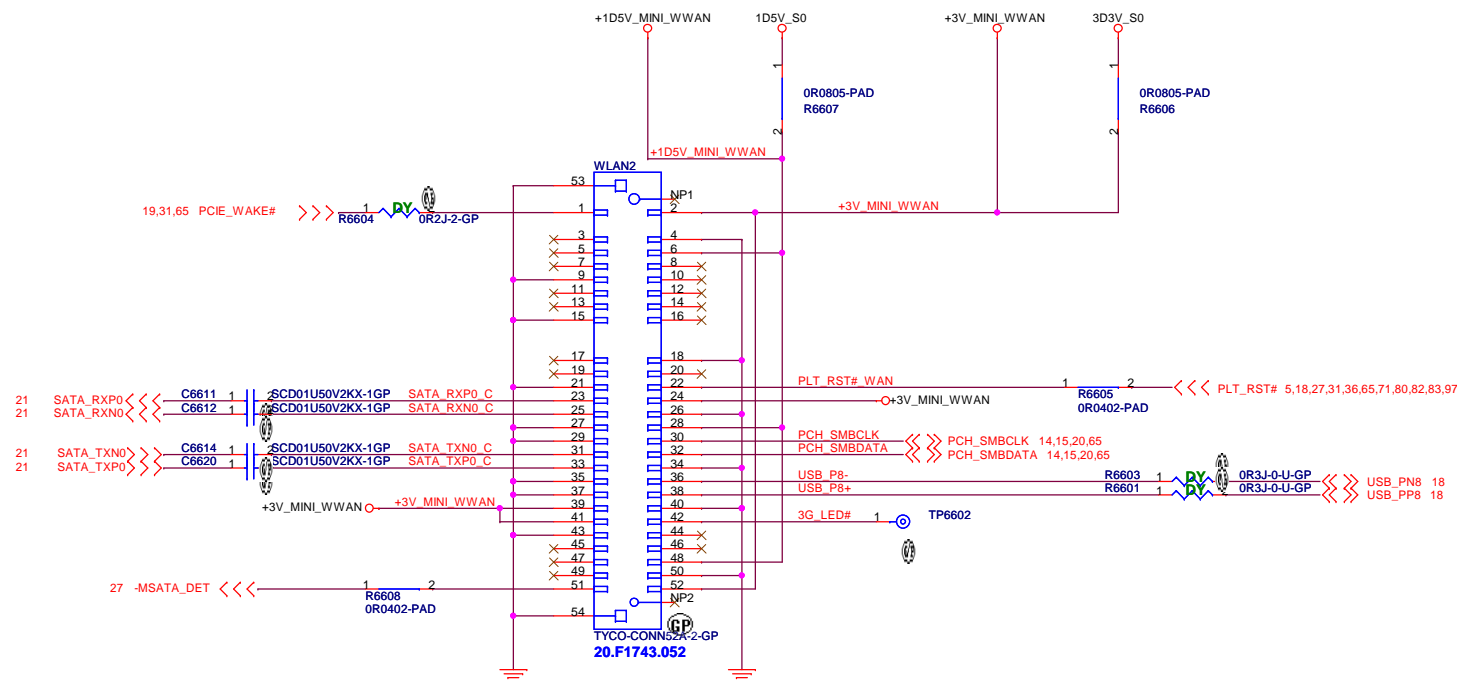
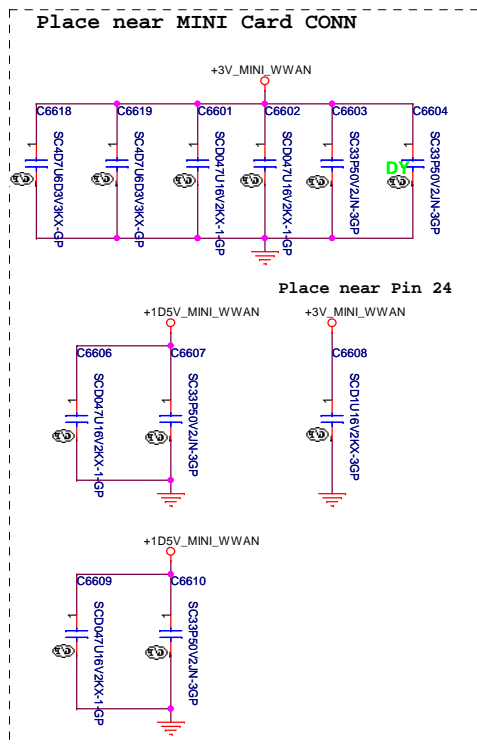
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN)/TP CONN
Size: A3 Document Number: LA480 Rev: SD
Date: Friday, January 06, 2012 Sheet: 65 of 103

SSID = Wireless

mSATA for V Series Only

Mini Card Connector(Full Card)



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

WWAN Connector

Size

Document Number

LA480

Rev

SD

Date: Friday, January 06, 2012

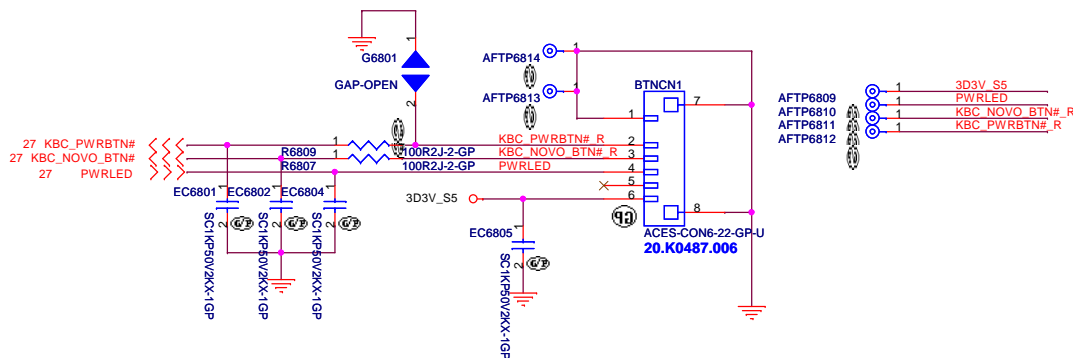
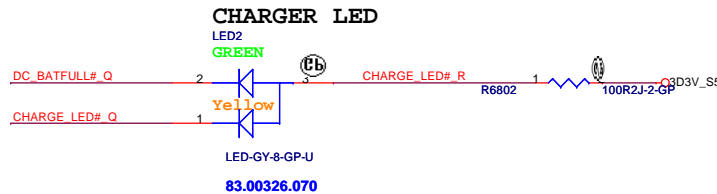
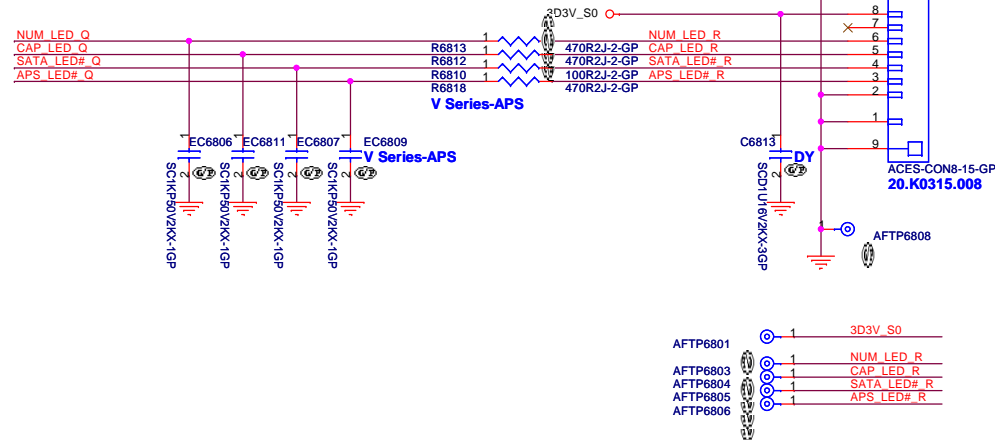
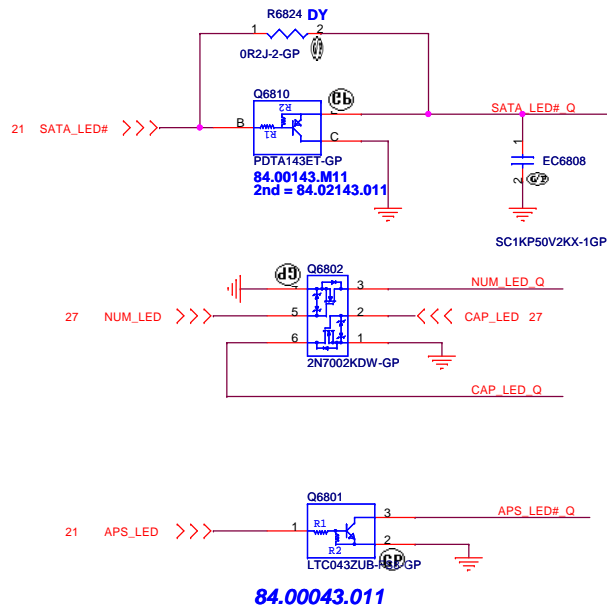
Sheet 66 of 103

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緯創資通		Wistron Corporation	
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Title			
Reserved			
Size	Document Number		Rev
A4	LA480		SD
Date:	Friday, January 06, 2012		Sheet 67 of 103

SSID = User.Interface

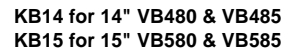


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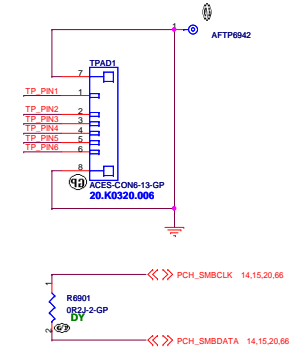
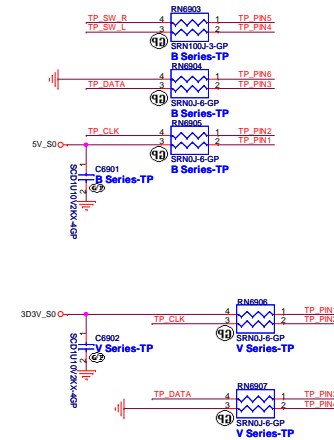
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		LED Bar/Power Button	
Size	Document Number	Rev	SD
A3	LA480	1	103
Date:	Friday, January 06, 2012	Sheet	68 of 103

Internal KeyBoard Connector




PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

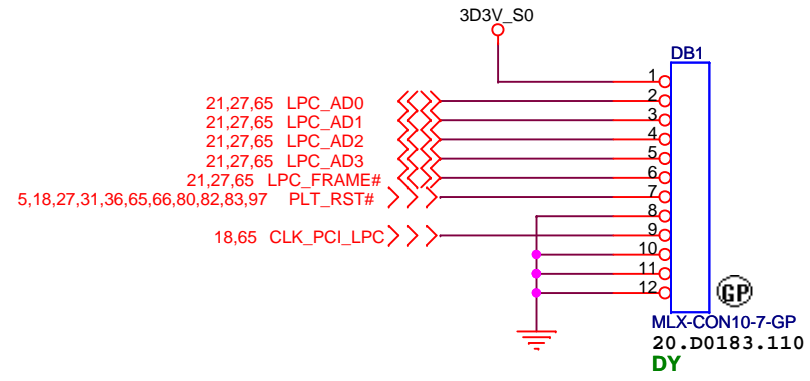


	Models			
Synaptics PIN	B480	V480	B580	V580
TM-01146-006	✓			
TM-02123-001		✓		
TM-02060-001			✓	
TM-02045-001				✓
VDD	5V	3.3V	5V	3.3V
Pin 1	VDD	VDD	VDD	VDD
Pin 2	CLK	CLK	CLK	CLK
Pin 3	DA7	DA7	DA7	DA7
Pin 4	Left button	GND	Right button	GND
Pin 5	Right button	NC	Left button	NC
Pin 6	GND	NC	Right button	NC



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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Hall Sensor			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 70 of	103



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Title

Dubug connector

Size

Document Number

LA480

Rev

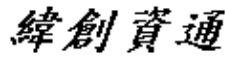
SD

Date: Friday, January 06, 2012

Sheet 71 of 103

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Title			
Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 72 of	103

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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	LA480		SD
Date:	Friday, January 06, 2012		Sheet 73 of 103

<Core Design>			
緯創資通		Wistron Corporation	
		21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsuehshien, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CARD Reader CONN			
Size	Document Number	Rev	
A2	LA480	SD	
Date	Friday, January 06, 2012	Sheet	74 of 103

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<Core Design>

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

New Card

Size

A4

Document Number

LA480

Rev

SD

Date: Friday, January 06, 2012

Sheet 75 of 103

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A4

Document Number

LA480

Rev

SD

Date: Friday, January 06, 2012

Sheet 76 of 103



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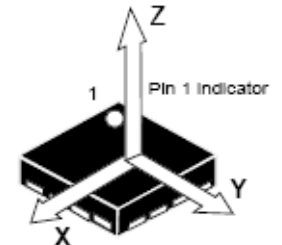
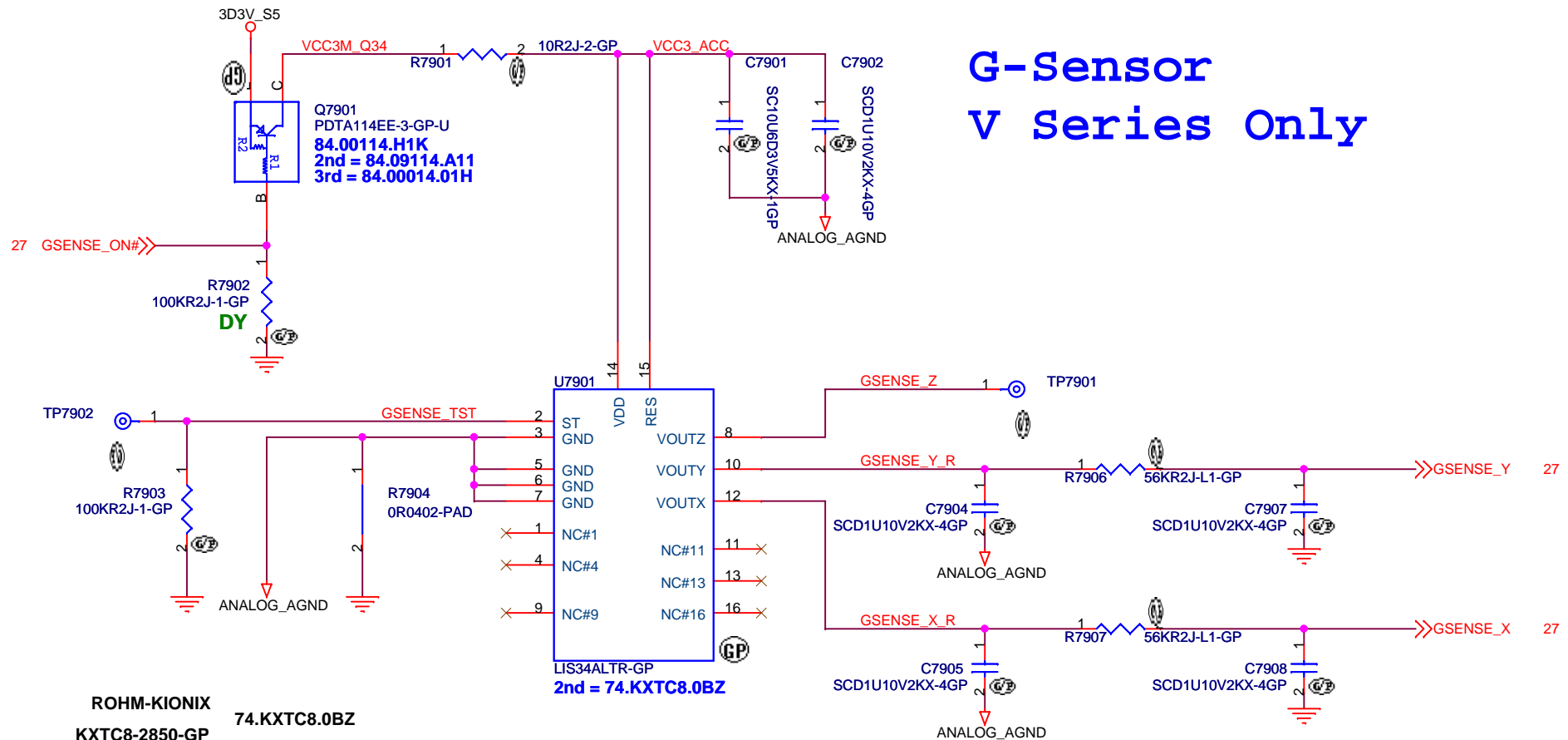
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Title <div>Reserved</div>	
Size <div>A4</div>	Document Number <div>LA480</div>
Date <div>Friday, January 06, 2012</div>	Rev <div>SD</div>
Sheet 77 of 103	

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	LA480		SD
Date:	Friday, January 06, 2012		Sheet 78 of 103

G-Sensor V Series Only



Layout Comment :

- (1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.
- (2) Avoid routing under DCDC switching area.

<Core Design>

緯創資通

Wistron Corporation

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Title

G-Sensor

Size A4 Document Number

LA480

Rev

SD

Date: Friday, January 06, 2012

Sheet 79 of 103

RFID

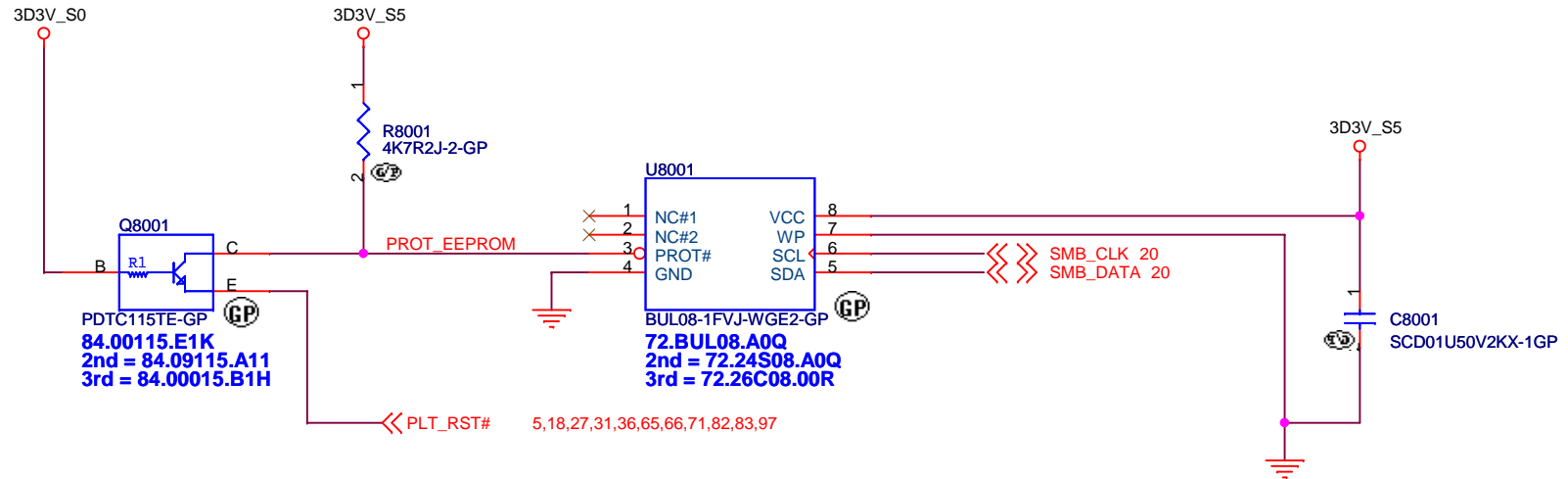



Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC115TE	N/A	84.00115.E1K
ROHM	LTC015TEB	N/A	84.00015.B1H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	N/A	72.BUL08.A0Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

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Title	
RF ID	
Size A4	Document Number LA480
Date: Friday, January 06, 2012	Rev SD
Sheet 80 of 103	

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Size

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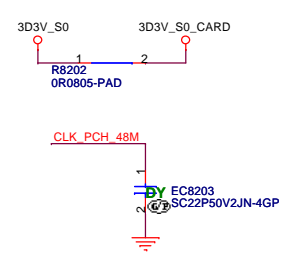
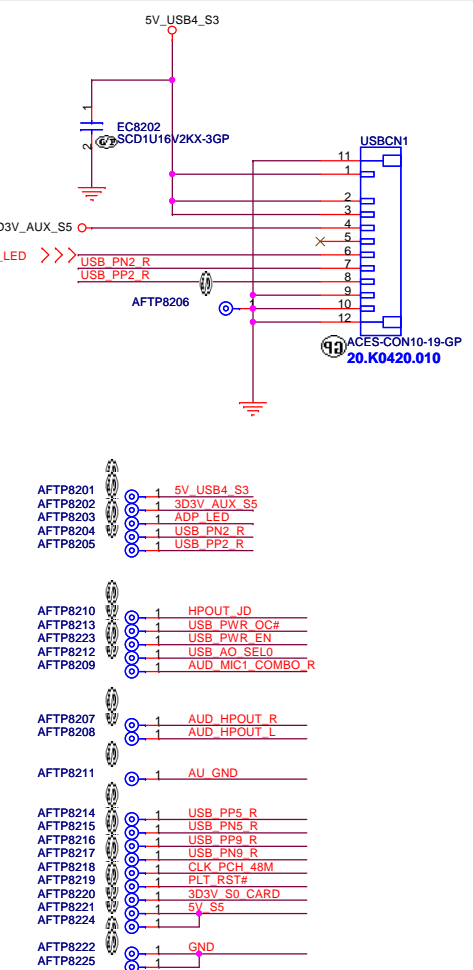
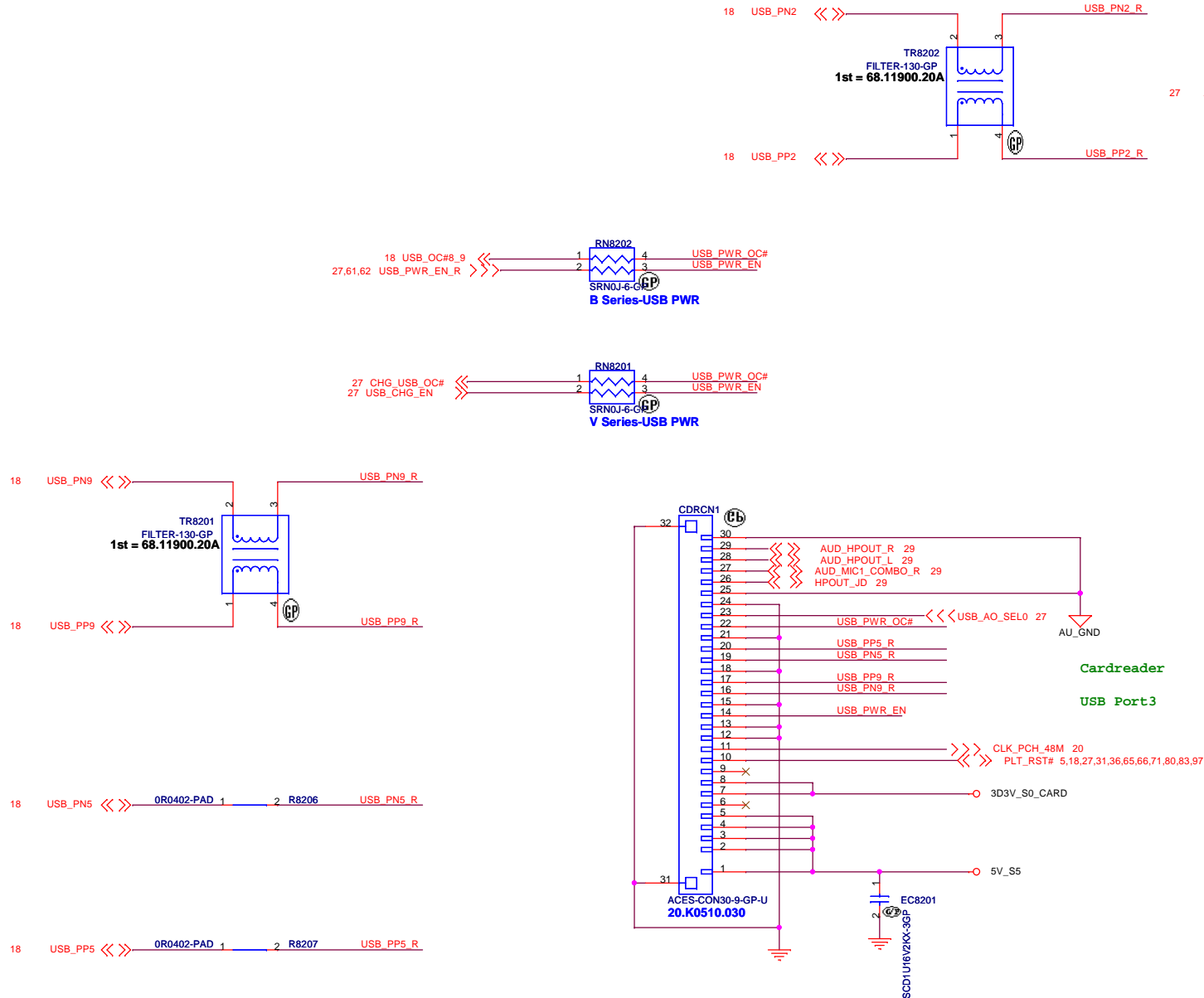
LA480

Rev

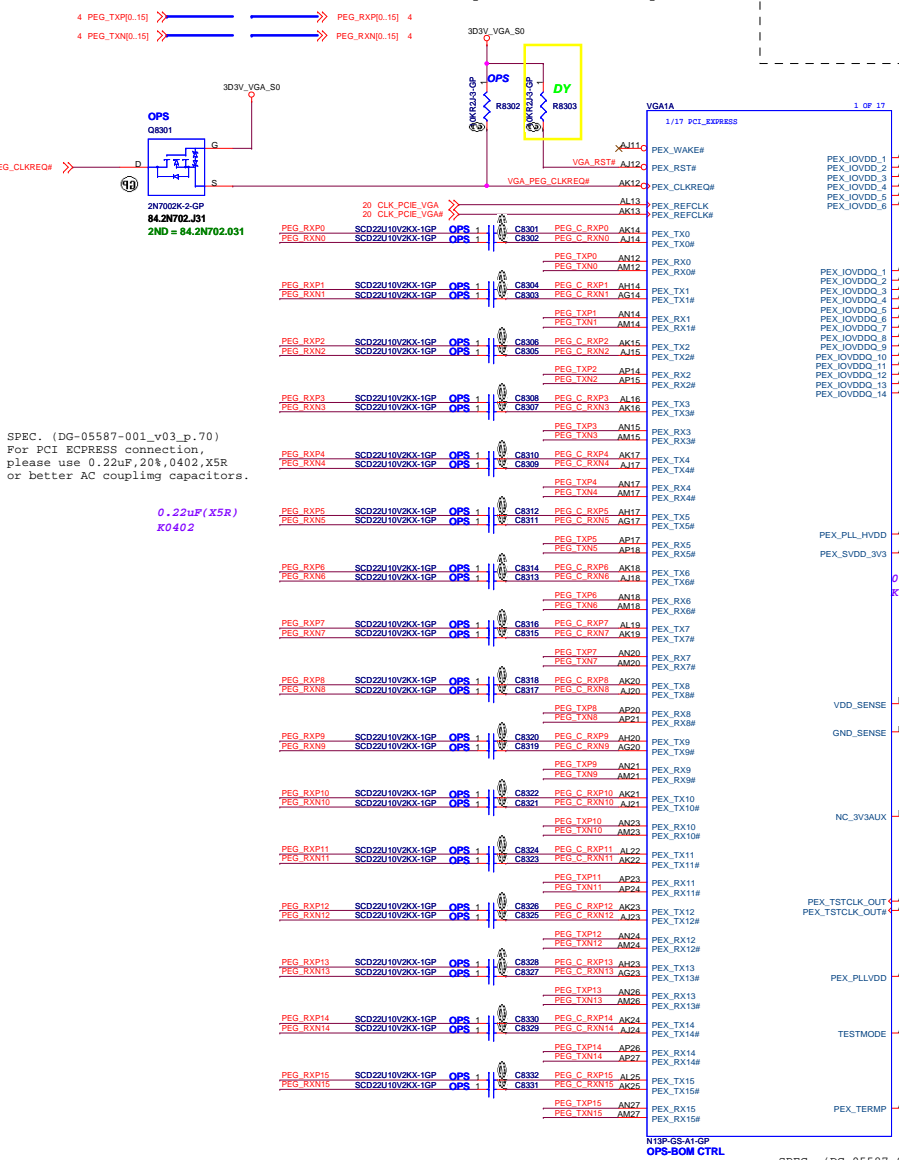
SD

Date: Friday, January 06, 2012

Sheet 81 of 103



SPEC. (DG-05587-001_v03_p.70)
 PEX_CLK_REQ_N is an open-drain bi-directional signal;
 by default it should have a 10 kΩ pull-up to 3.3V.
 This signal is an active low signal.



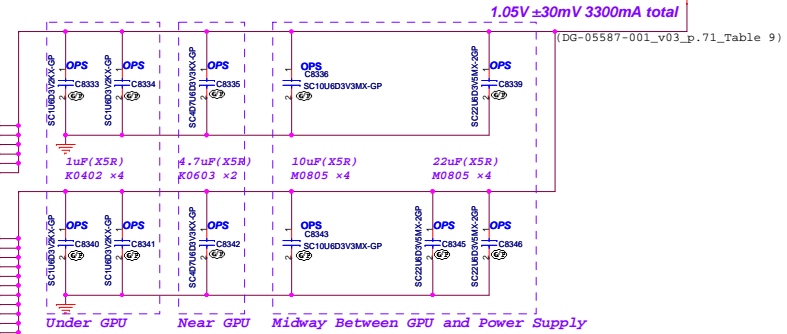
SPEC. (DG-05587-001_v03_p.70)
 For PCI ECPRESS connection,
 please use 0.22uF, 20%, 0402, X5R
 or better AC coupling capacitors.

0.22uF(X5R)
 K0402

PCI Express PEX_IOVVD/Q Combined (DG-05587-001_v03_p.72_Table 10)

Capacitor Type	Footprint	Population	Location
1.0uF	X6S	0402	4
4.7uF	X6S	0603	2
10uF	X5R	0805	4
22uF	X5R	0805	4

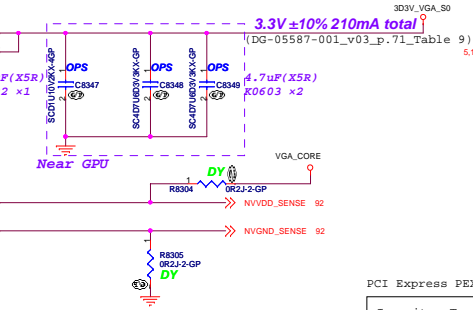
X6S (+/-22% -55-105°C)
 X5R (+/-15% -55-85°C)



PCI Express PEX_SVDD/PLLHVDD Connected to NV3V3 (DG-05587-001_v03_p.72_Table 12)

Capacitor Type	Footprint	Population	Location
0.1uF	X5R	0402	1
4.7uF	X5R	0603	2

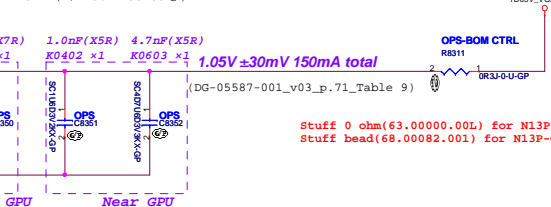
X5R (+/-15% -55-85°C)



PCI Express PEX_PLLVDD (DG-05587-001_v03_p.72_Table 11)

Capacitor Type	Footprint	Population	Location
100nF	X6S	0402	1
1.0uF	X5R	0603	1
4.7uF	X5R	0805	1

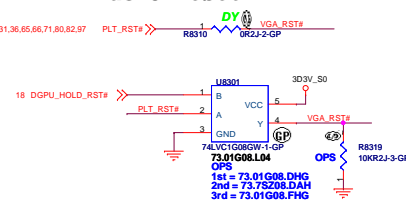
X6S (+/-22% -55-105°C)
 X5R (+/-15% -55-85°C)



SPEC. (DG-05587-001_v03_p.214)
 By default, pull-down the TESTMODE pin to GND with a 10kΩ resistor.
 For XOR tree testing, TESTMODE should be pulled up to 3v3 with a 10 kΩ resistor.

SPEC. (DG-05587-001_v03_p.70)
 PEX_TERM is used for internal calibration;
 pull-down this signal with 2.49 kΩ, 1% resistor.

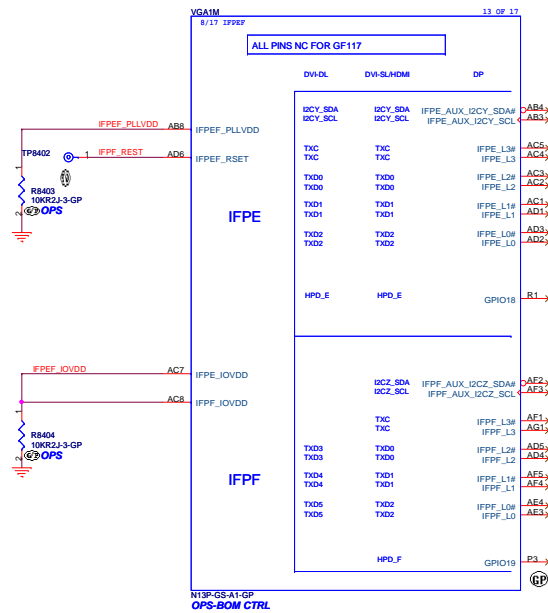
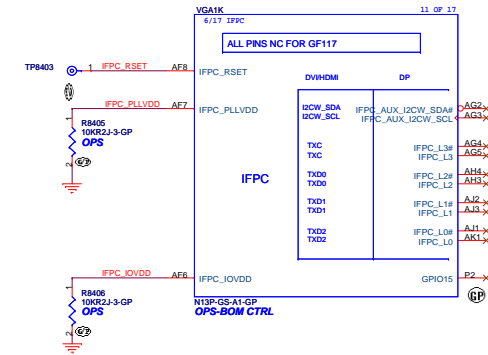
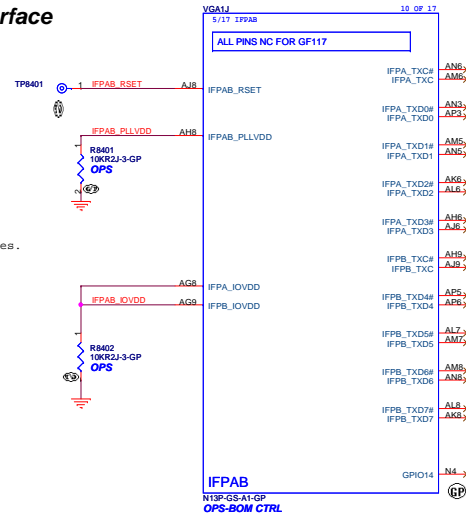
dGPU reset



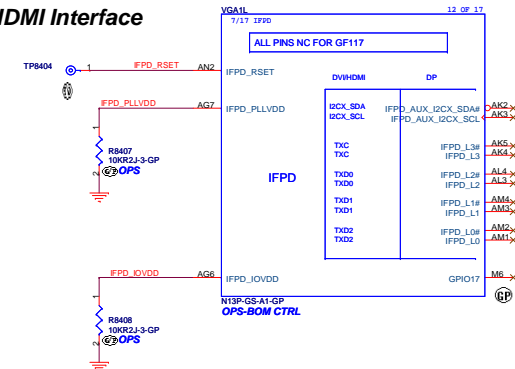
Stuff 0 ohm(63.00000.00L) for N13P-GS/N13M-GS,
 Stuff bead(68.00082.001) for N13P-GL/N13M-GE

LVDS Interface

SPEC. (DG-05587-001_v03_p.160)
Pull down IFPxy IOVDD with 10kΩ resistor.
Pull down IFPxy PLLVDD with 10kΩ resistor.
The other IO pins can be NC, this includes unused data lines.



HDMI Interface

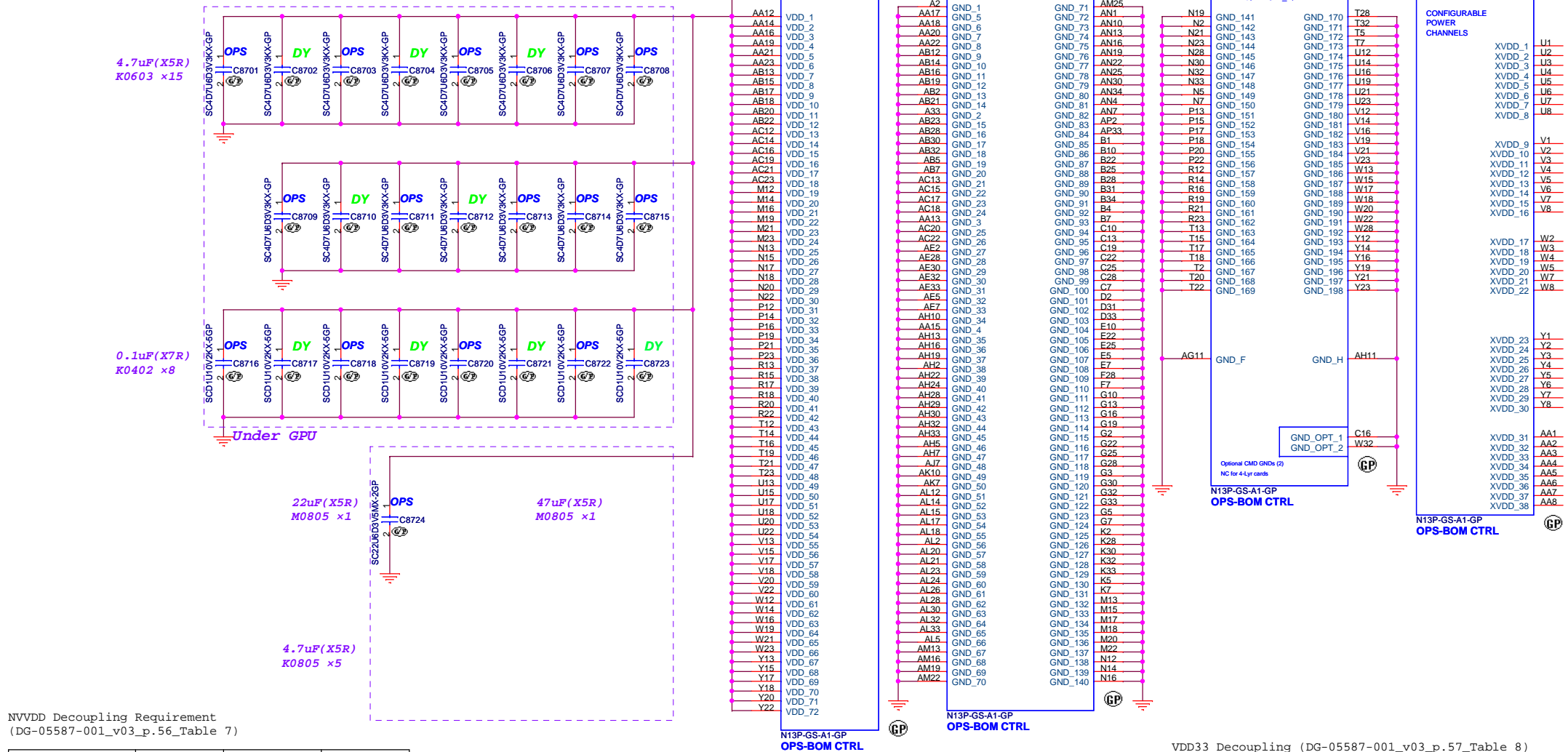


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Taipei Hsin 221, Taiwan, R.O.C.

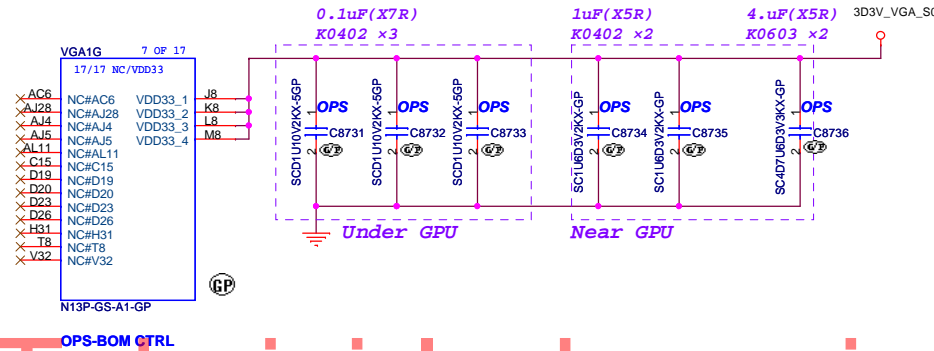
Title N13P_GPU (2/5): DIGITALOUT
Size A0 Document Number LA48 Rev SD
Date Friday, January 05, 2012 Sheet 84 of 103





Capacitor Type	Footprint	Population	Location
4.7uF	X6S	0603	15
0.1uF	X7R	0402	8
47uF	X5R	0805	1
22uF	X5R	0805	1
4.7uF	X5R	0805	5

X7R (+/-15%、-55~125°C)
X6S (+/-22%、-55~105°C)
X5R (+/-15%、-55~85°C)



VDD33 Decoupling (DG-05587-001_v03_p.57_Table 8)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	3
1uF	X5R	0402	2
4.7uF	X5R	0603	1

X7R (+/-15%、-55~125°C)
X5R (+/-15%、-55~85°C)

<Core Design>

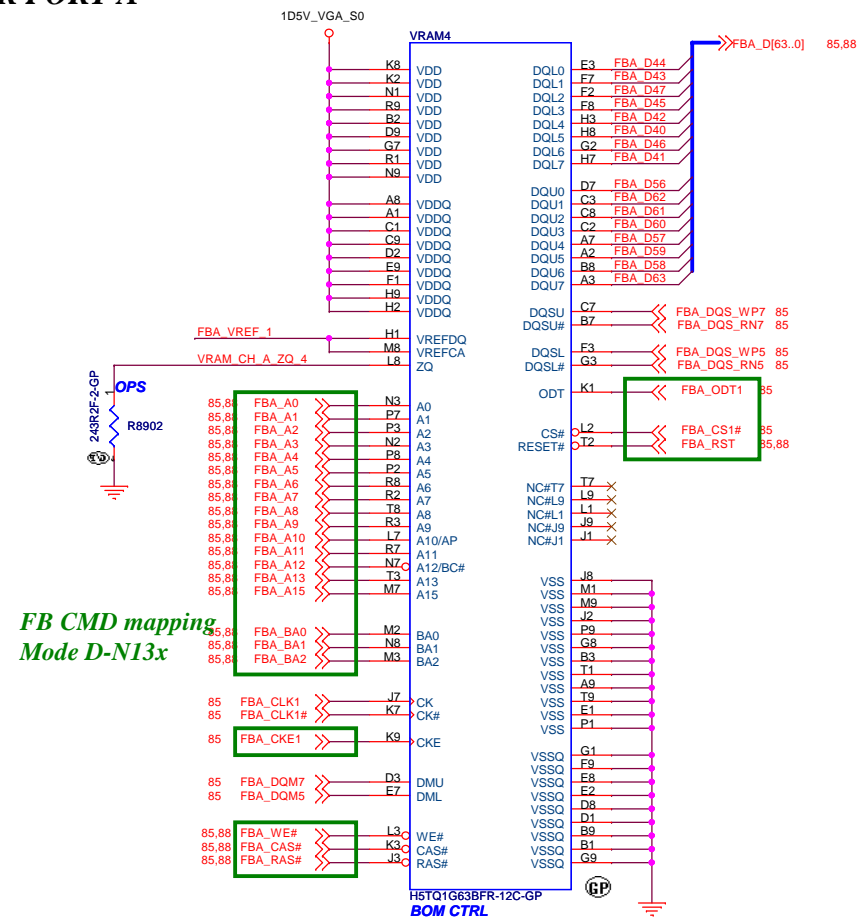
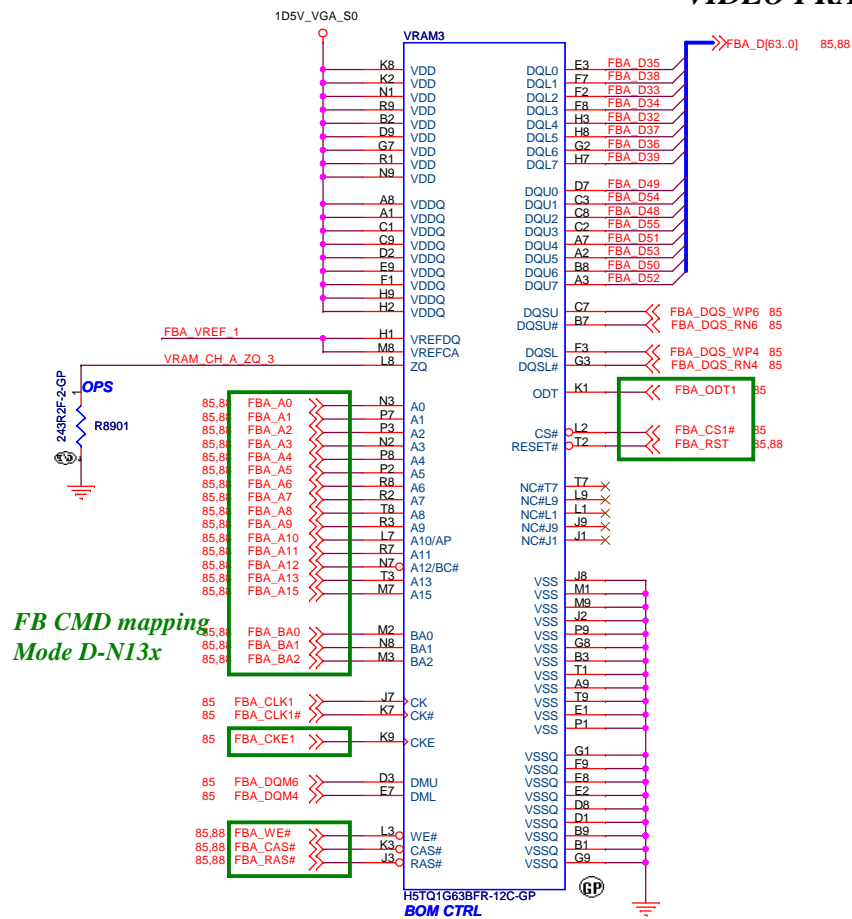
緯創資通 Wistron Corporation
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File: **N13P GPU (5/5): PWR/GND**

Size: **A3** Document Number: **LA48** Rev: **SD**

Date: Friday, January 06, 2012 Sheet 87 of 103

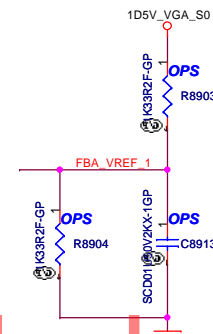
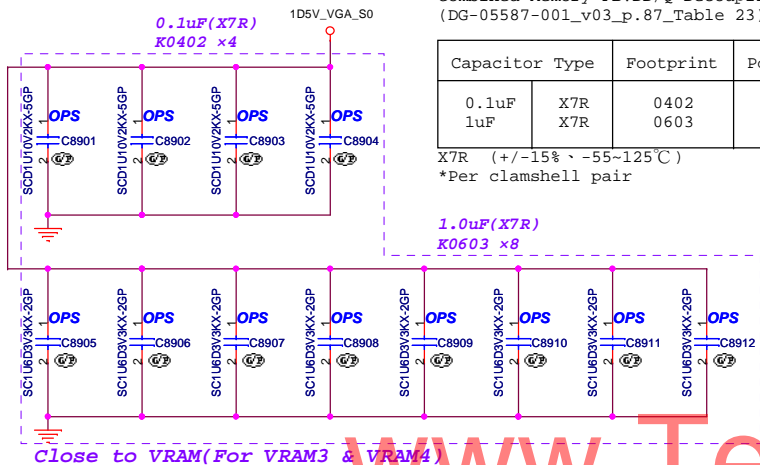
VIDEO FRAME BUFFER PORT A



Combined Memory FBVDD/Q Decoupling DDR3x16 with Clamshell Layout (DG-05587-001_v03_p.87_Table 23)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	Close to VRAM
1uF	X7R	0603	Close to VRAM

X7R (+/-15%、-55-125°C)
*Per clamshell pair



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Title CHANNEL-A_VRAM3,4 (2/4)

Size A3 Document Number

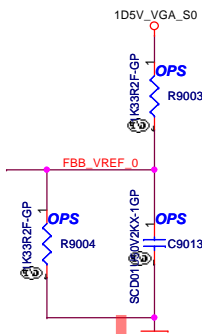
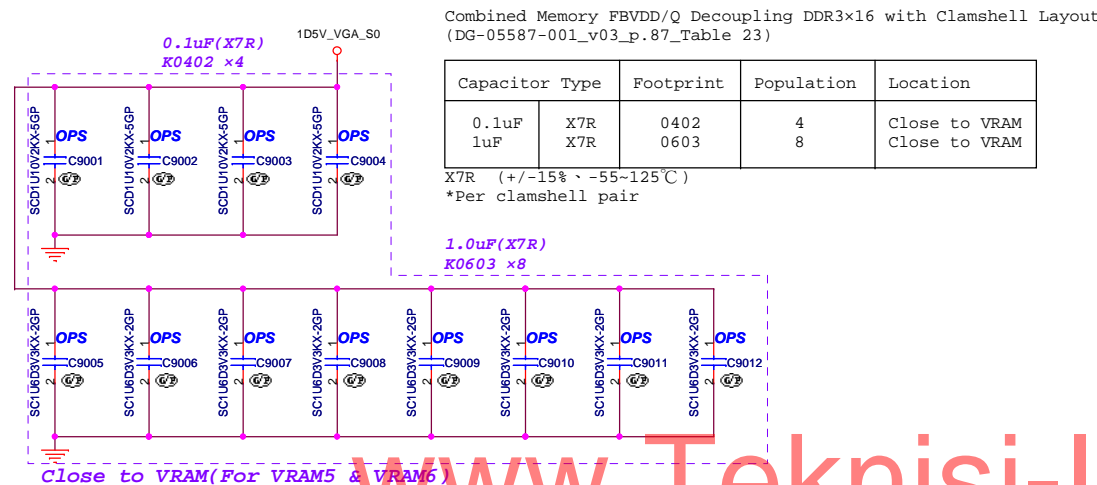
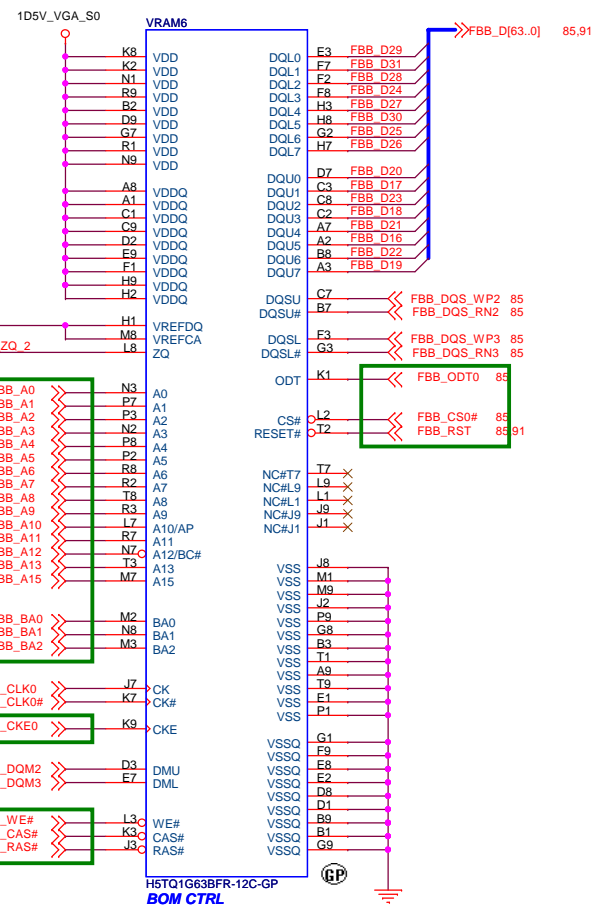
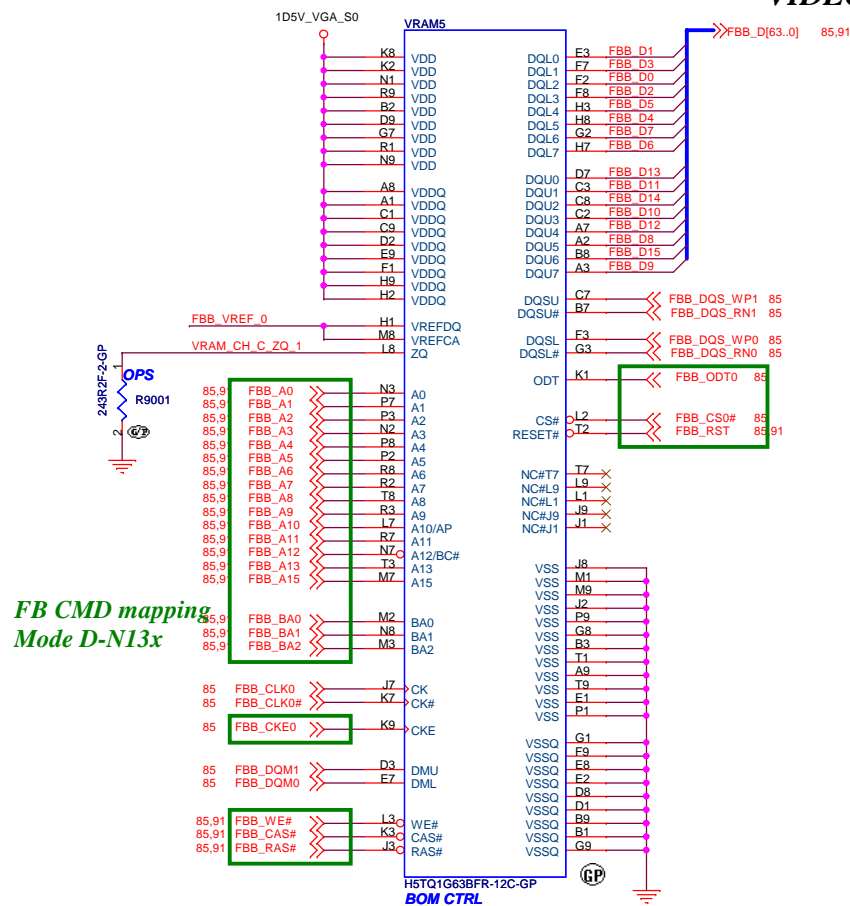
LA48

Date: Friday, January 06, 2012

Sheet 89 of 103

Rev SD

VIDEO FRAME BUFFER PORT C



<Core Design>

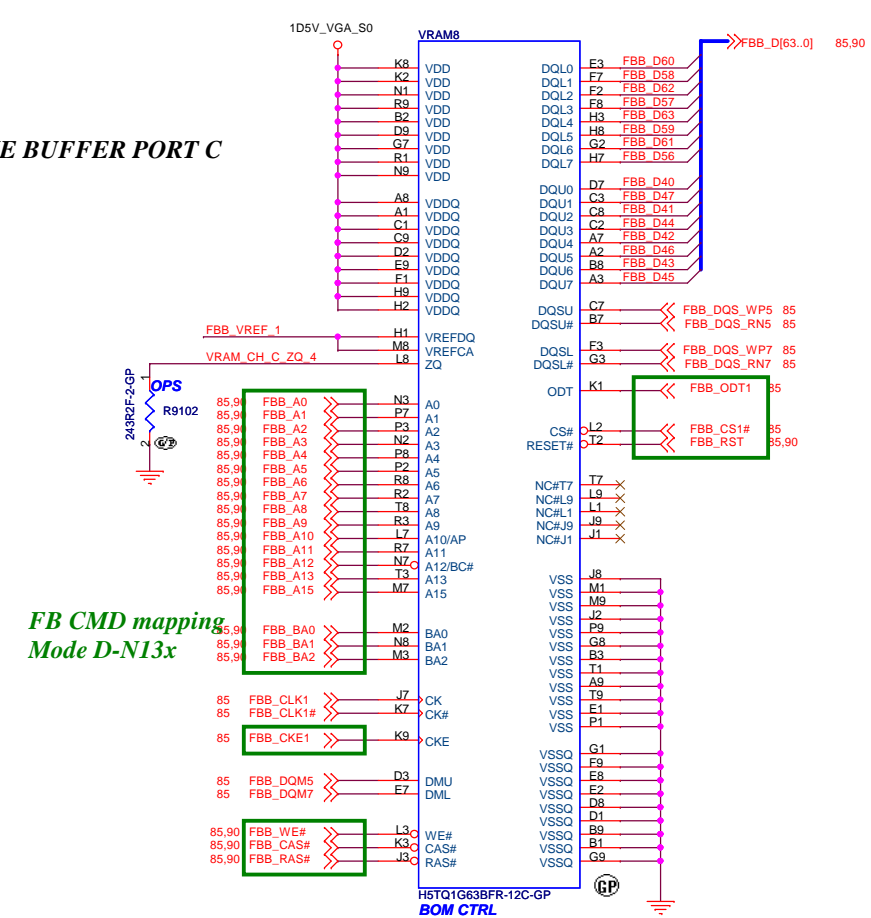
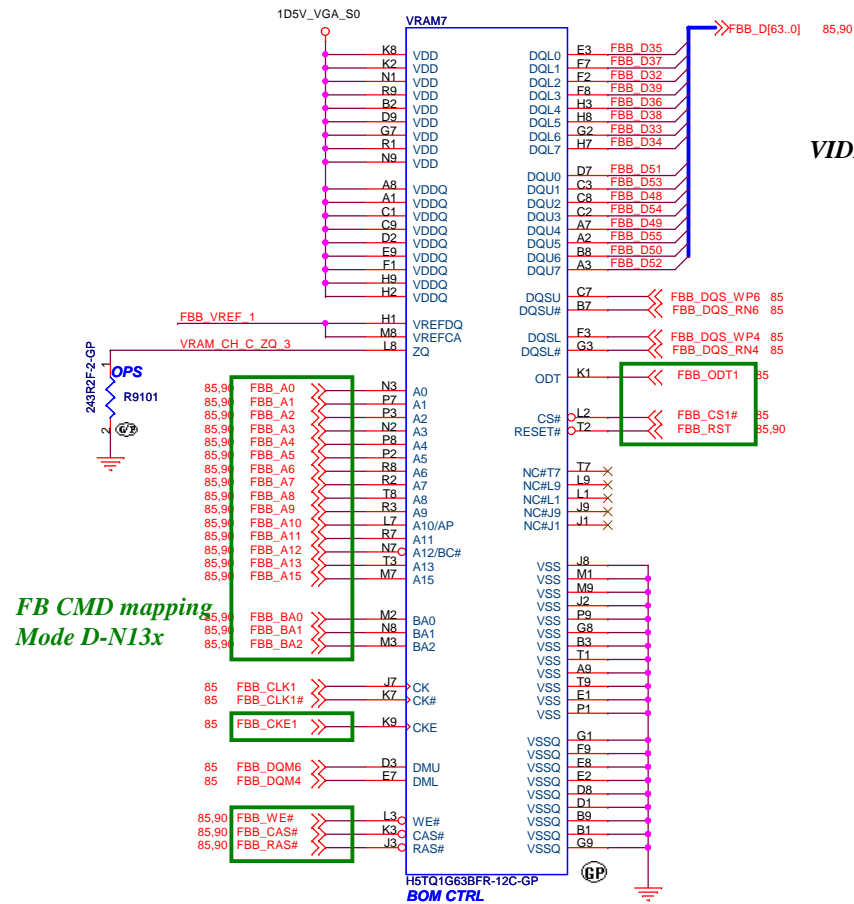
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Title: **CHANNEL-C_VRAM5,6 (3/4)**

Size: A3 Document Number: **LA48** Rev: **SD**

Date: Friday, January 06, 2012 Sheet: 90 of 103

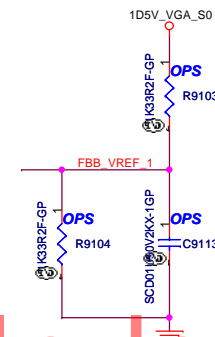
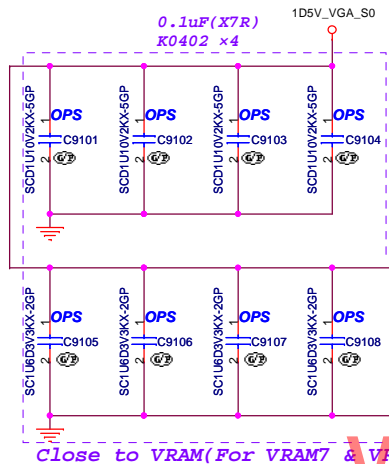
VIDEO FRAME BUFFER PORT C



Combined Memory FBVDD/Q Decoupling DDR3x16 with Clamshell Layout (DG-05587-001_v03_p.87_Table 23)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	4
1uF	X7R	0603	8

X7R (+/-15%、-55-125°C)
*Per clamshell pair



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Title CHANNEL-C_VRAM7,8 (4/4)

Size A3 Document Number

LA48

Date: Friday, January 06, 2012

Sheet 91 of 103

Rev SD

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Size A4	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 94	of 103

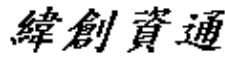
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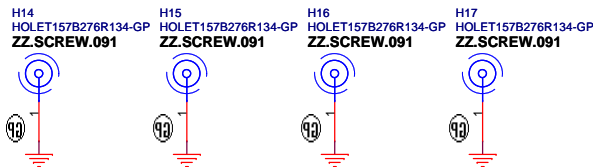
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Size	Document Number		Rev
A4	LA480		SD
Date:	Friday, January 06, 2012		Sheet 95 of 103

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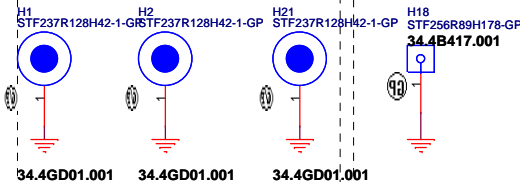
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TOUCH PANEL			
Size	Document Number		Rev
A4	LA480		SD
Date: Friday, January 06, 2012		Sheet 96 of	103

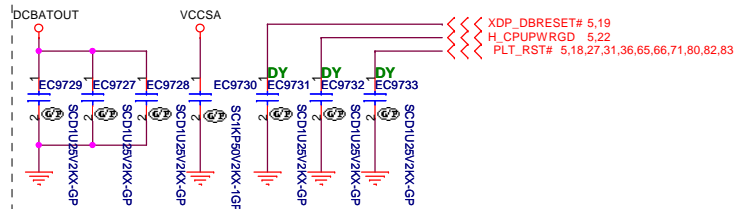
CPU Plate



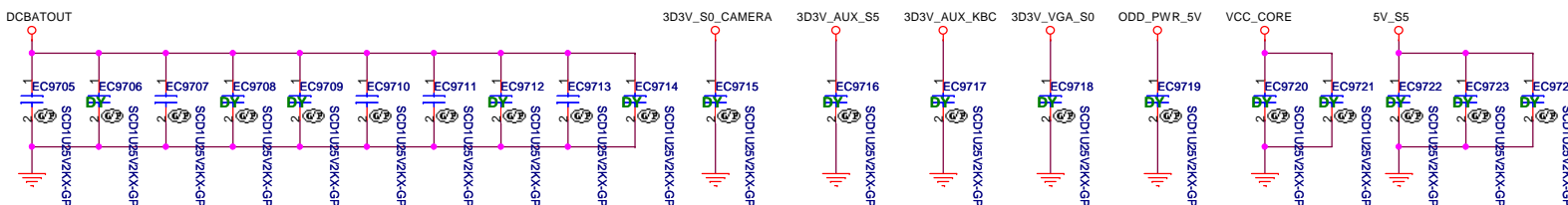
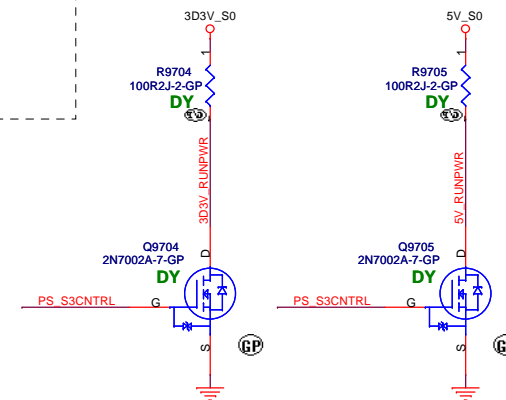
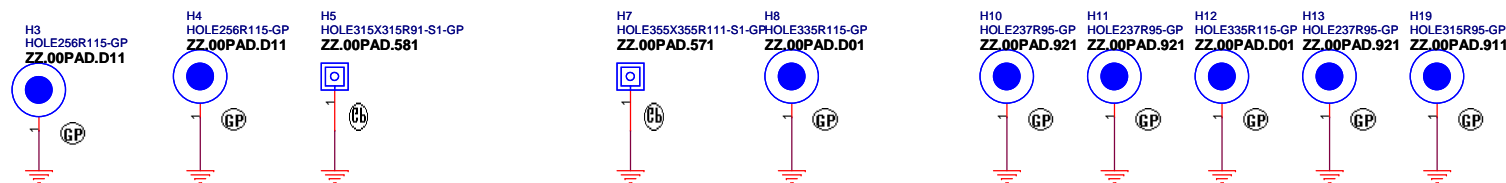
VGA Std-Off



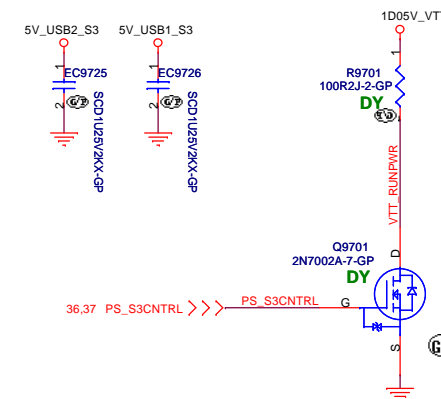
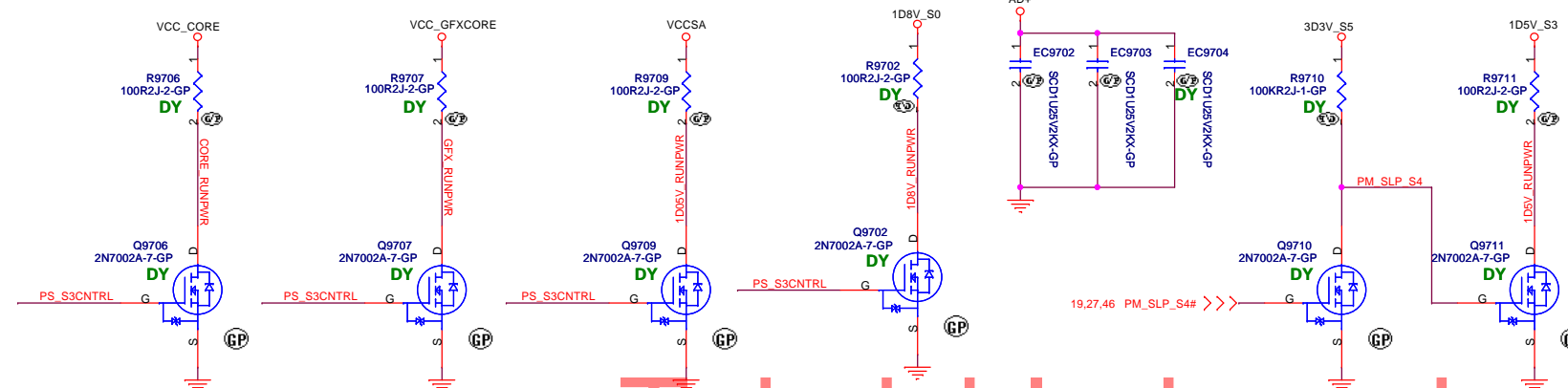
MINI PCIE



14" Structure boss



For Discharge



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Title			
UNUSED PARTS/EMI Capacitors			
Size	Document Number	Rev	
A3	LA480	SI	
Date:	Friday, January 06, 2012	Sheet 97 of	103

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Size

Document Number

Rev

A4

LA480

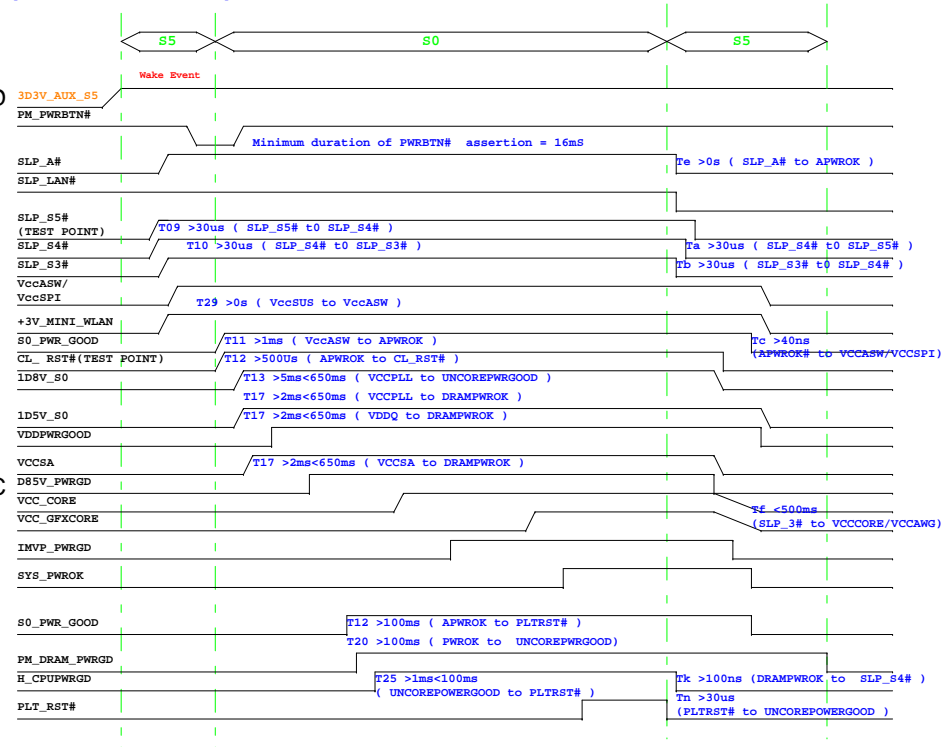
SD

Date: Friday, January 06, 2012

Sheet 98 of 103

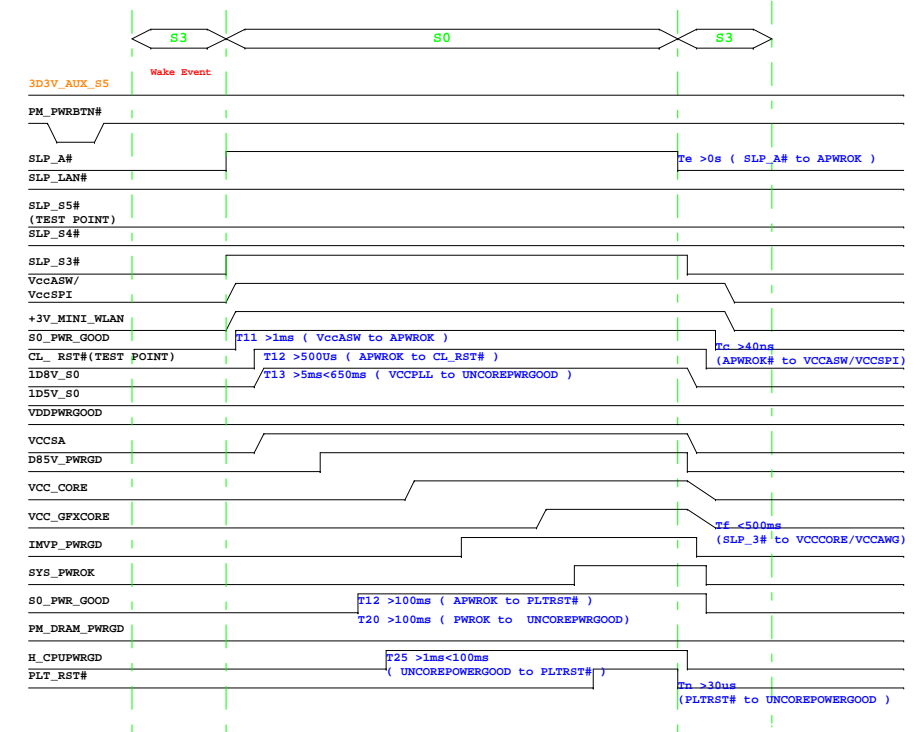
Intel-Power Sequence

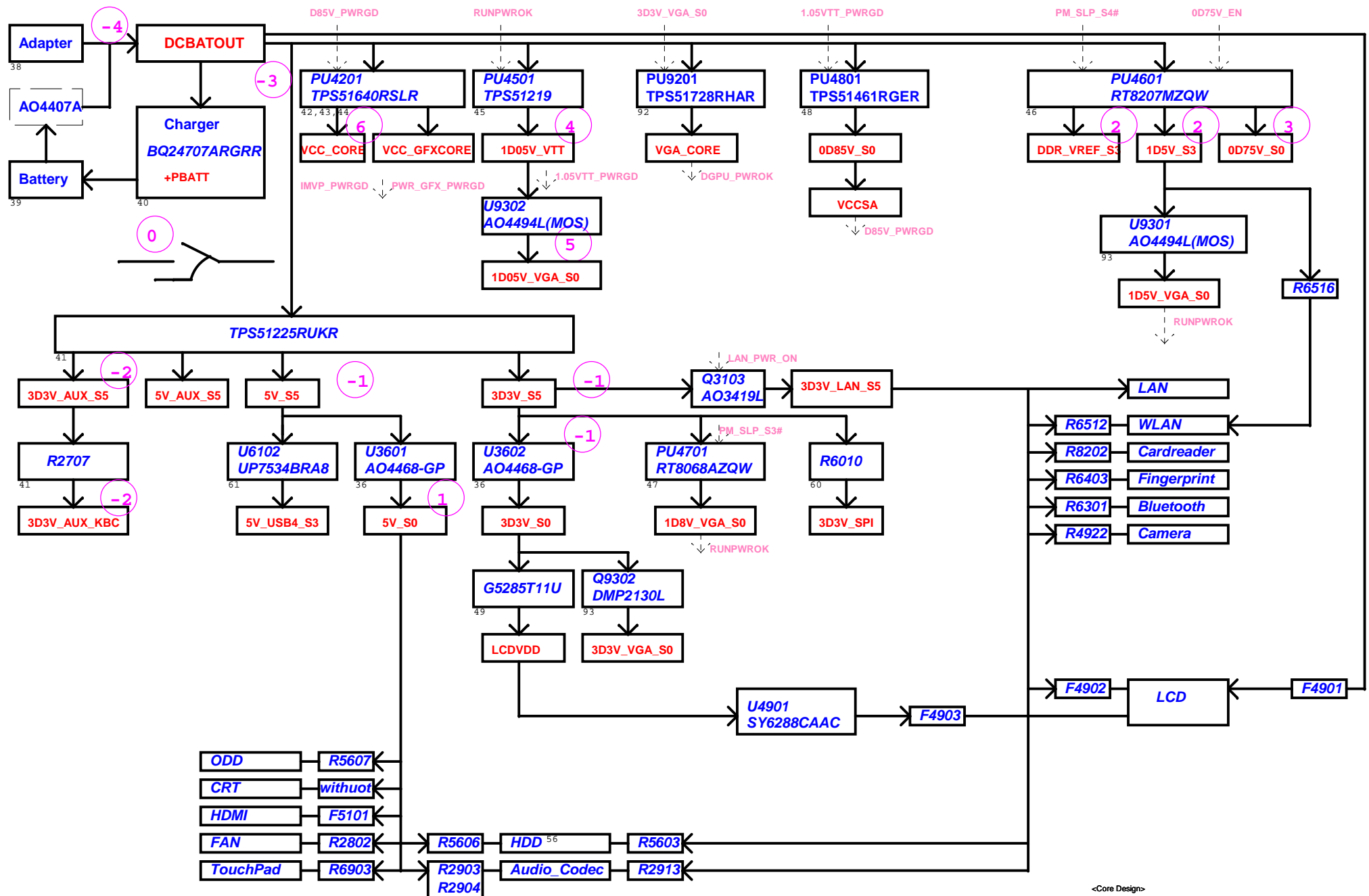
(S5-to-S0-to-S5)



Intel PCH Pin Name	Main board PCH Pin Name
VccSUS (5V/3V)	3D3V_AUX_S5
PWRBTN#	PM_PWRBTN#
SLP_A#	SLP_A#
SLP_LAN#	SLP_LAN#
SLP_S5#	PM_SLP_S5#
SLP_S4#	PM_SLP_S4#
SLP_S3#	PM_SLP_S3#
VccASW/VccSPI	VccASW/VccSPI
Vcc_WLAN	+3V_MINI_WLAN
PWROK/APWROK	S0_PWR_GOOD
CL_RST#	CL_RST#
VCCPLL	ID8V_S0
VDDQ	ID5V_S0
VR_VDDQ_PWRGOOD	VDDPWRGOOD
VCCSA	VCCSA
IMVP7_VR_EN	D85V_PWRGD
VccCore	VCC_CORE
VccAGX	VCC_GFXCORE
IMVP7_PWRGD	IMVP_PWRGD
SYS_PWRGD	SYS_PWRGD
PWROK	S0_PWR_GOOD
DRAM_PWRGD	PM_DRAM_PWRGD
UNCORE_PWRGD	H_CPUPWRGD
PLTRST#	PLT_RST#

(S3-to-S0-to-S3)



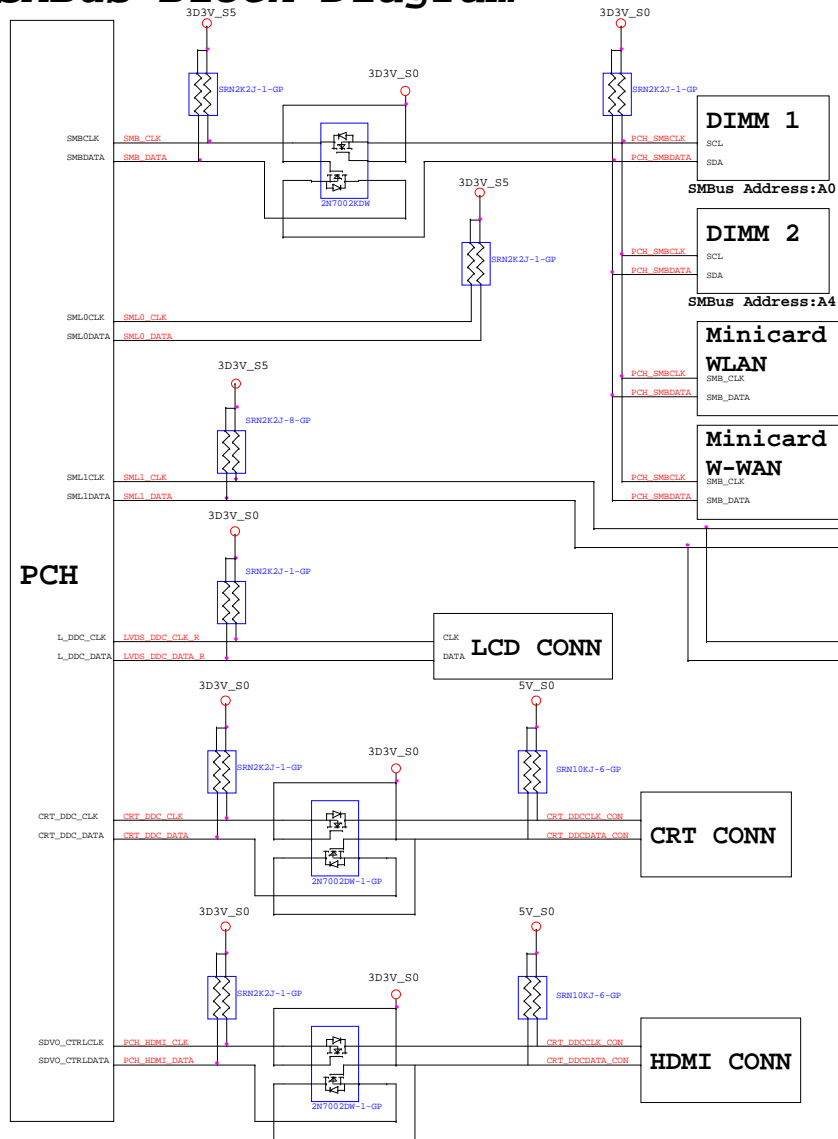


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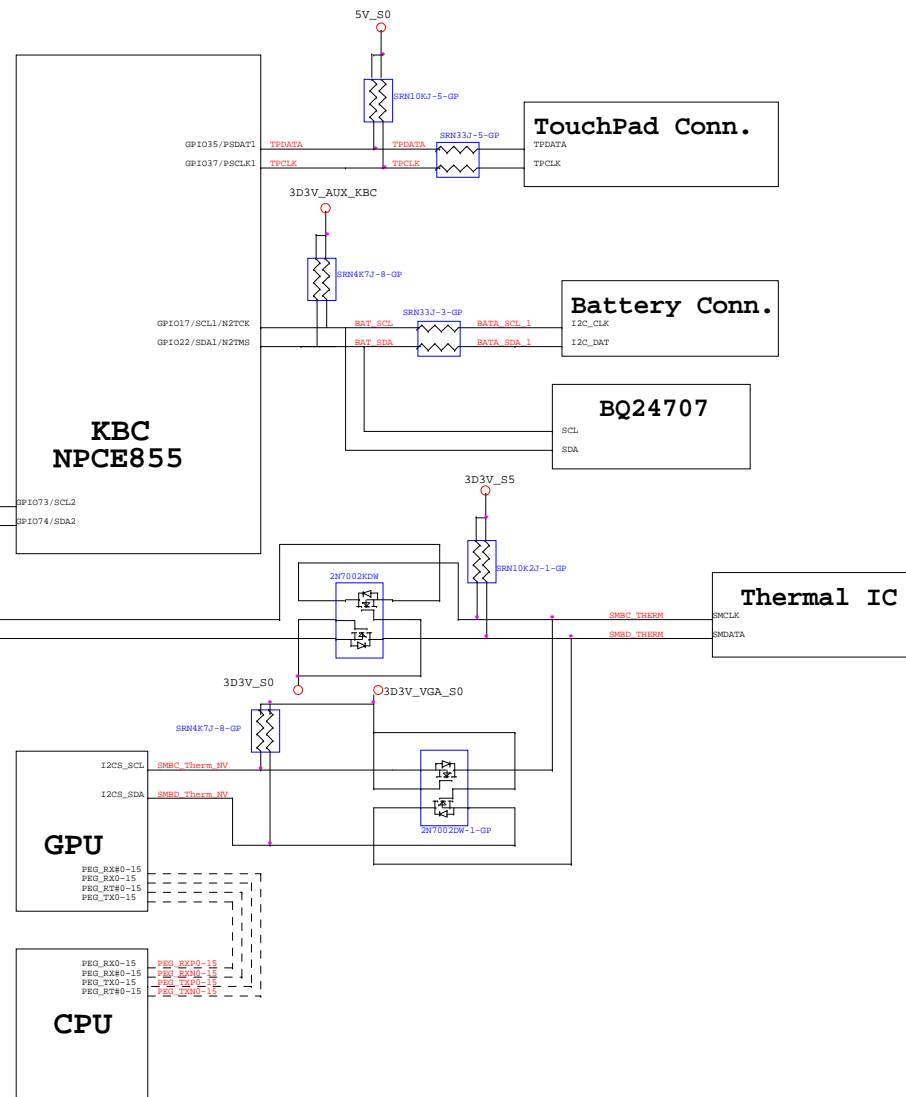
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Title		
Power Block Diagram		
Size	Document Number	Rev
A3	LA480	SD
Date	Friday, January 06, 2012	Sheet 100 of 103

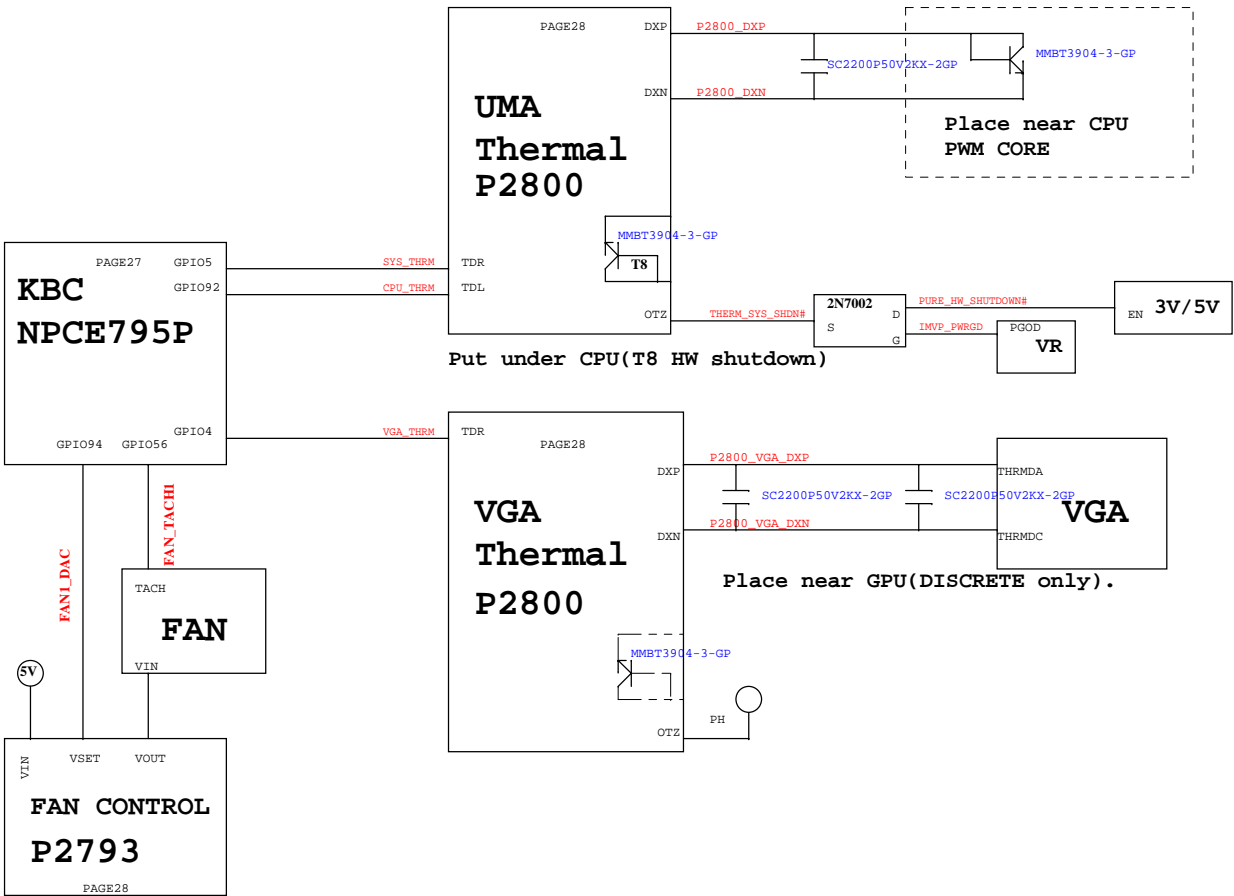
PCH SMBus Block Diagram



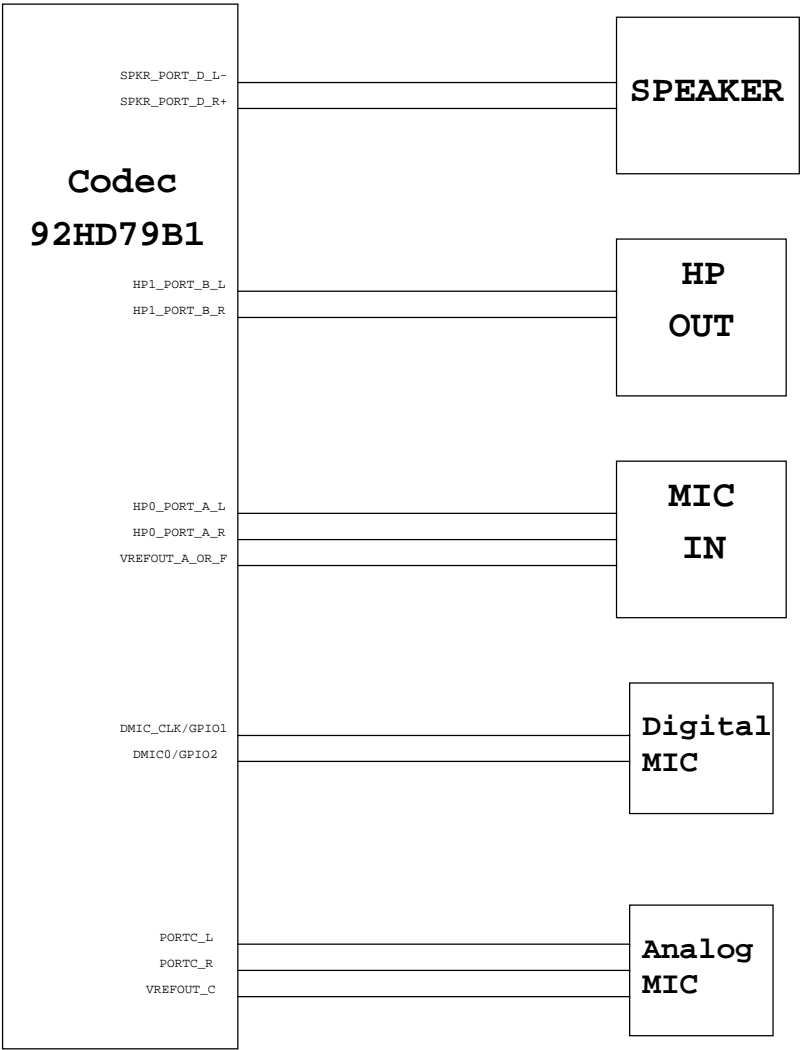
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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Size

Document Number

Rev

A4

LA480

SD

Date: Friday, January 06, 2012

Sheet 103 of 103